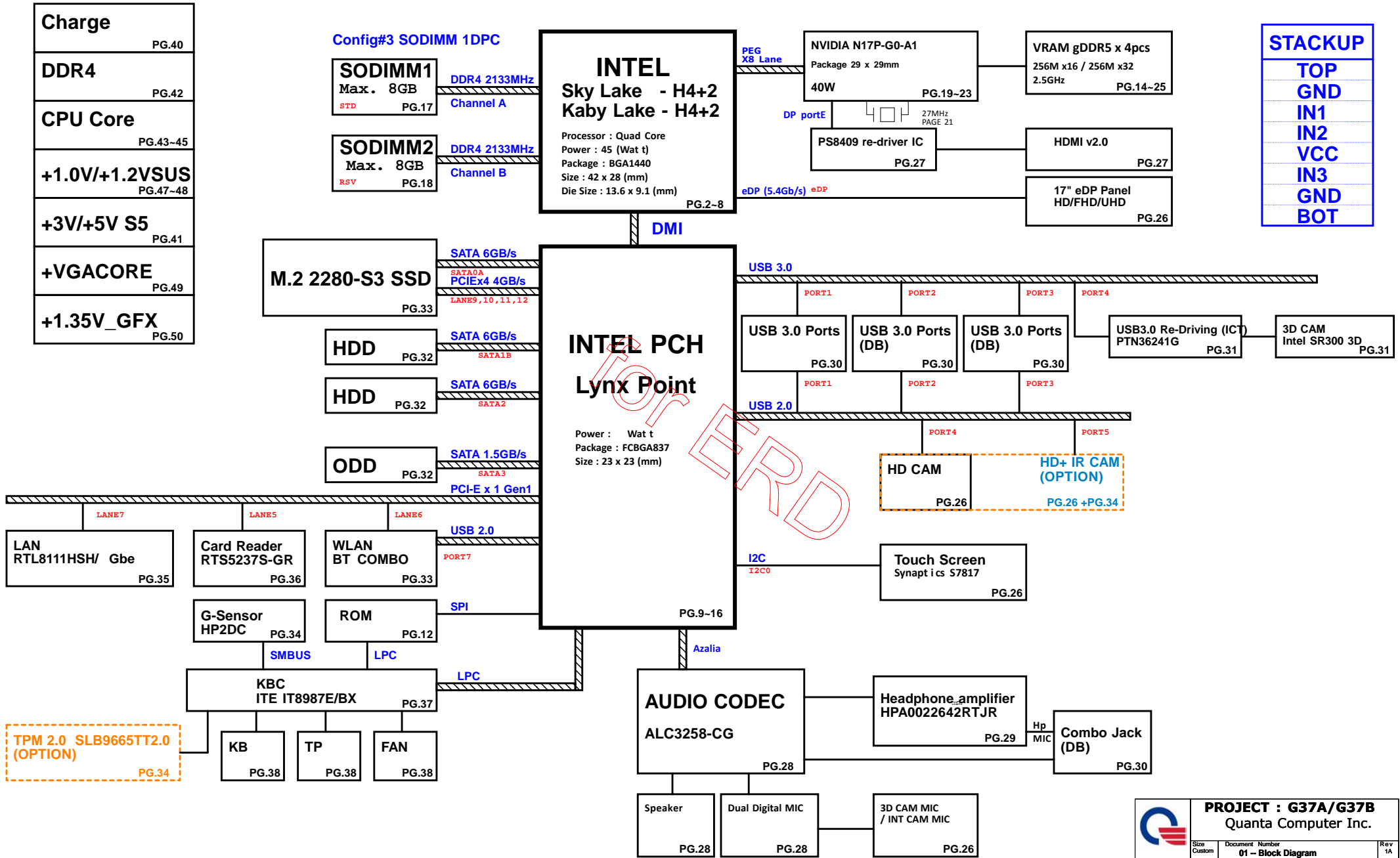
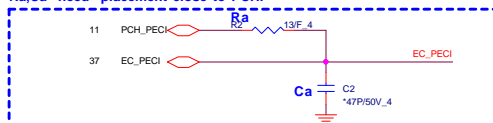


# POWER PAVILION PARFAIT INTEL SKL / KABY -H SYSTEM DIAGRAM 01

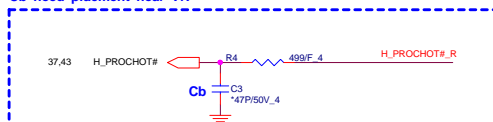


+1.0V 5.6,10,16,37,48  
+VCCSTPLL 6,43,47

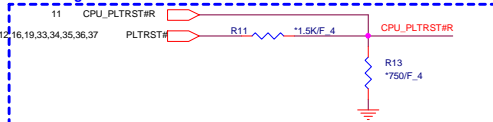
H\_PECI (50ohm)  
Trace Length: <0.5 inches  
Ra,Ca need placement close to PCH.



PROCHOT# (50ohm)  
Trace Length <11 inches  
Cb need placement near VR

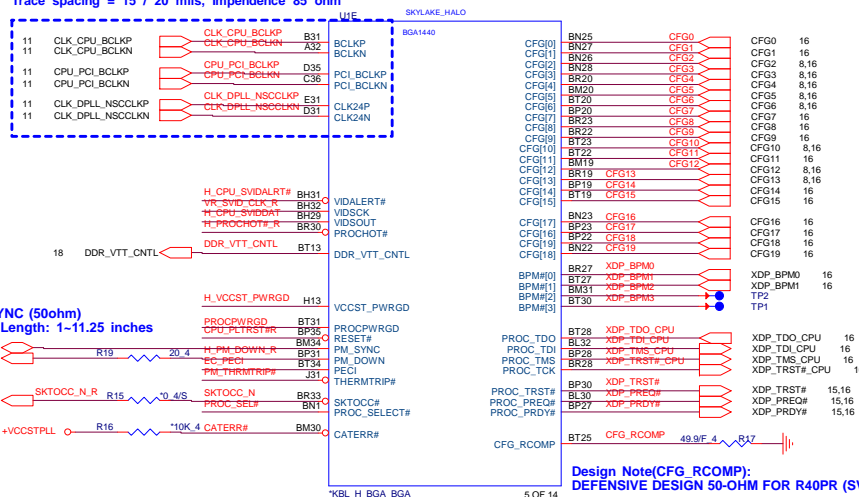


CPU\_PLTRST# (50ohm)  
Trace Length: 10-17 inches

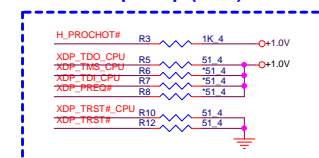


## Kaby Lake Processor (CLK,MISC,JTAG)

Host CLK:  
Trace length < 11000 mils  
Trace spacing = 15 / 20 mils, Impedance 85 ohm



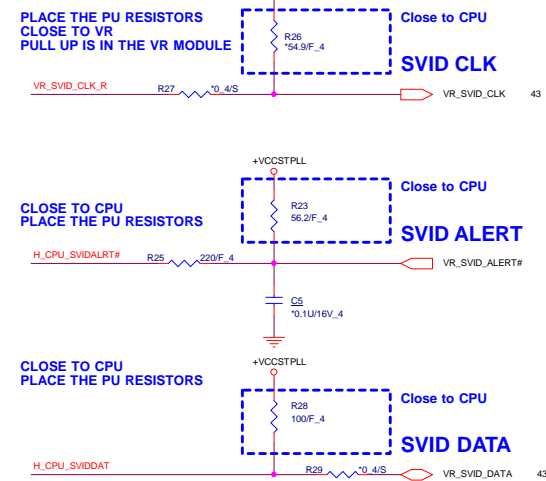
## Processor pull-up (CPU)



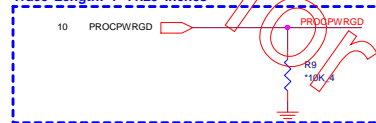
Design Note(CFG\_RCOMP):  
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

## CPU CORE SVID

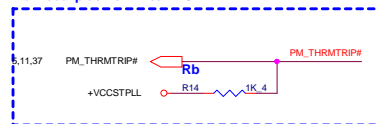
Layout note:  
1.Need routing together  
2.ALERT need between CLK and DATA.



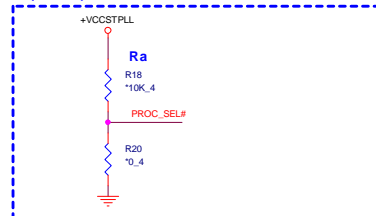
PROCPWRGD (50ohm)  
Trace Length: 1-11.25 inches



THERMTRIP# (50ohm)  
Trace Length: 1.1-12 inches  
Rb need placement near PCH

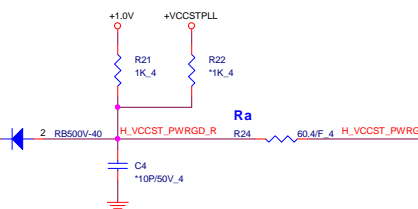


Ra(R10804) Not install in SKL-H



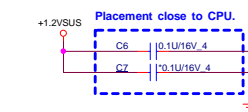
## HWRPD

Ra close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"

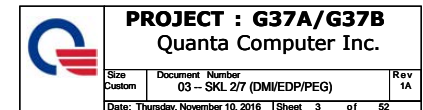


## CPU VDDQ

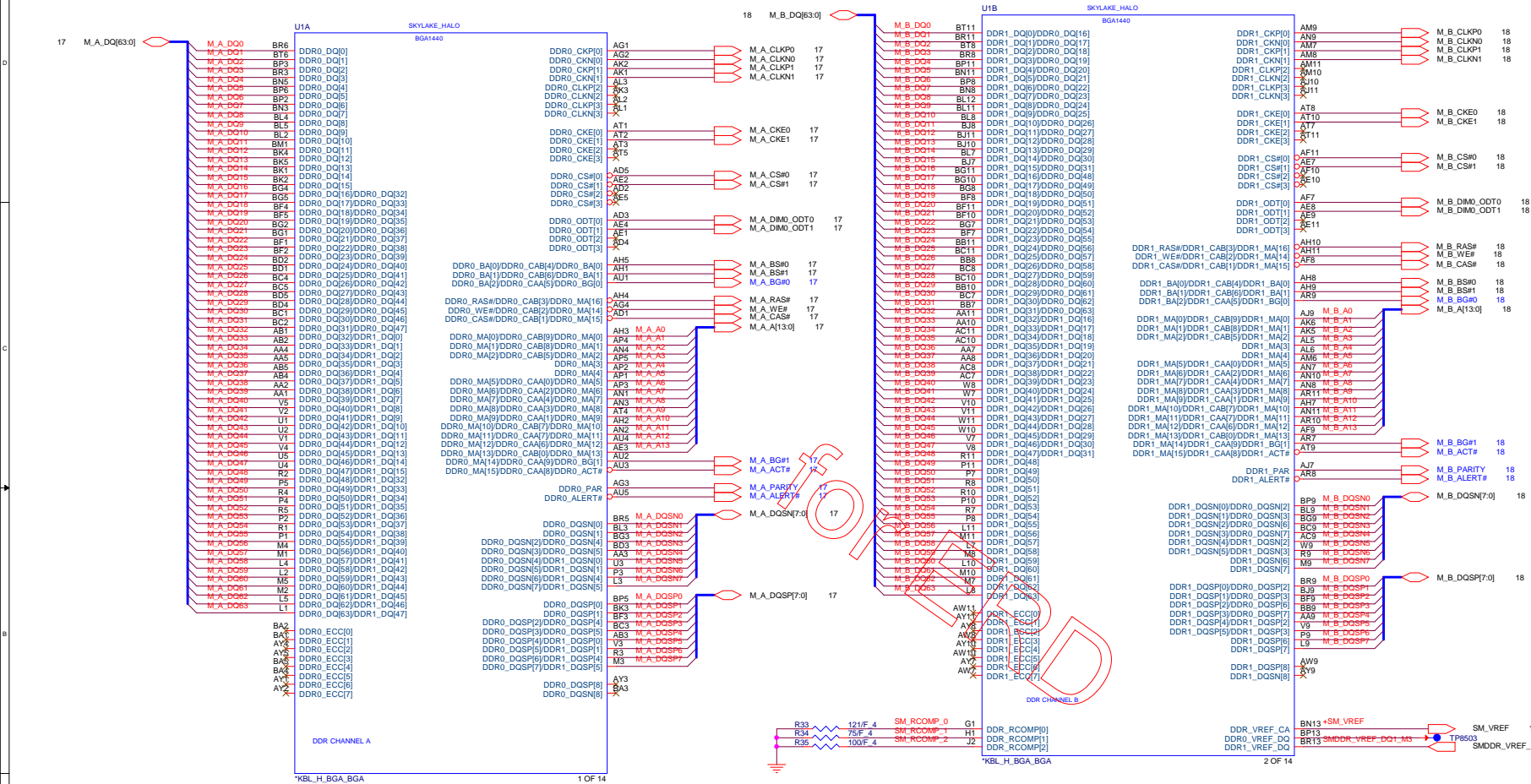
Note: please keep plane is enough for VDDQ 2.8A



|                                   |   |           |
|-----------------------------------|---|-----------|
| PROJECT : G37A/G37B               |   |           |
| Quanta Computer Inc.              |   |           |
| Size<br>Custom                    | Document Number<br>02 - SKL 1/7 (JTAG/MISC) | Rev<br>1A |
| Date: Thursday, November 10, 2016 | Sheet                                       | 2 of 82   |



## Kaby Lake Processor (DDR4)



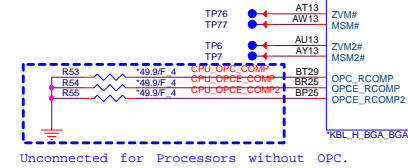
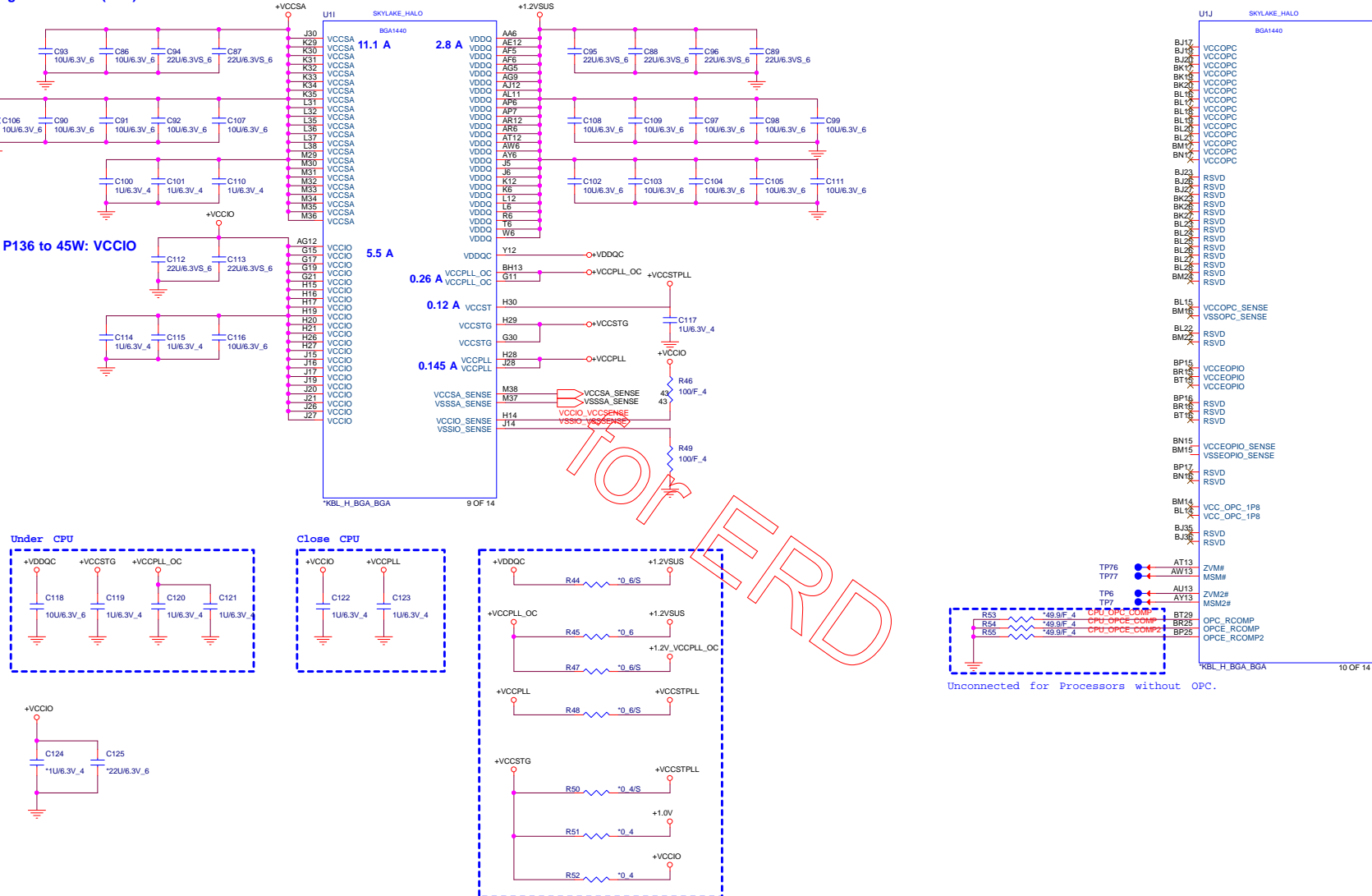



+1.2VSUS 2,10,17,18,42,48,51  
 +VCCIO 3,16,48  
 +VCCSTPLL 2,43,47  
 +VCCSA 43,45

Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow SKL H EDS page 135 45W: VDDQ=2.8A

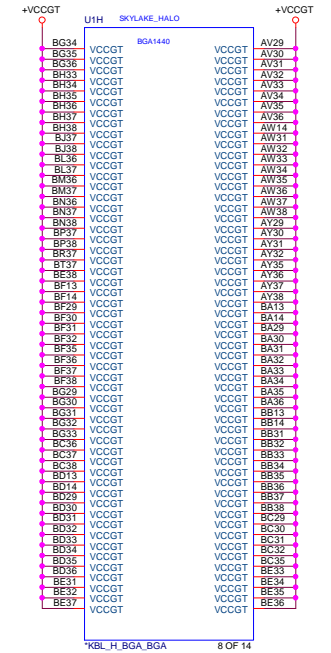
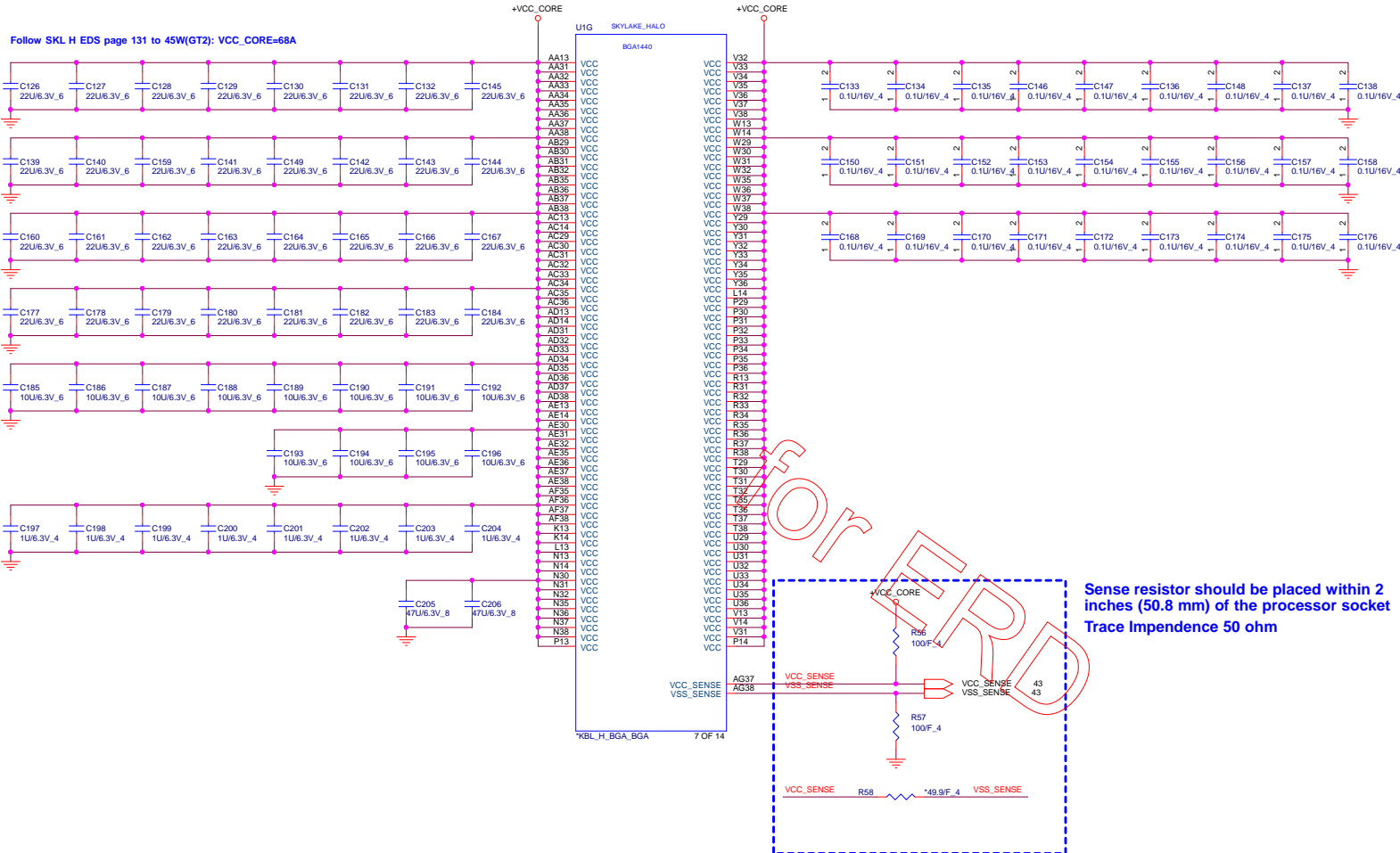
Follow SKL H EDS P136 to 45W: VCCIO  
+VCCIO = 0.95V



|   |   |           |
|---|---|-----------|
|  <b>PROJECT : G37A/G37B</b><br><b>Quanta Computer Inc.</b> |   |           |
| Size<br>Custom  | Document Number<br>06 - SKL 5/7 (POWER&GND) | Rev<br>1A |
| Date: Thursday, November 16, 2016   Sheet 6 of 52   |   |           |

+VCC\_CORE 44  
+VCCGT 5,43,45

Follow SKL H EDS page 131 to 45W(GT2): VCC\_CORE=68A



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket  
Trace Impedance 50 ohm

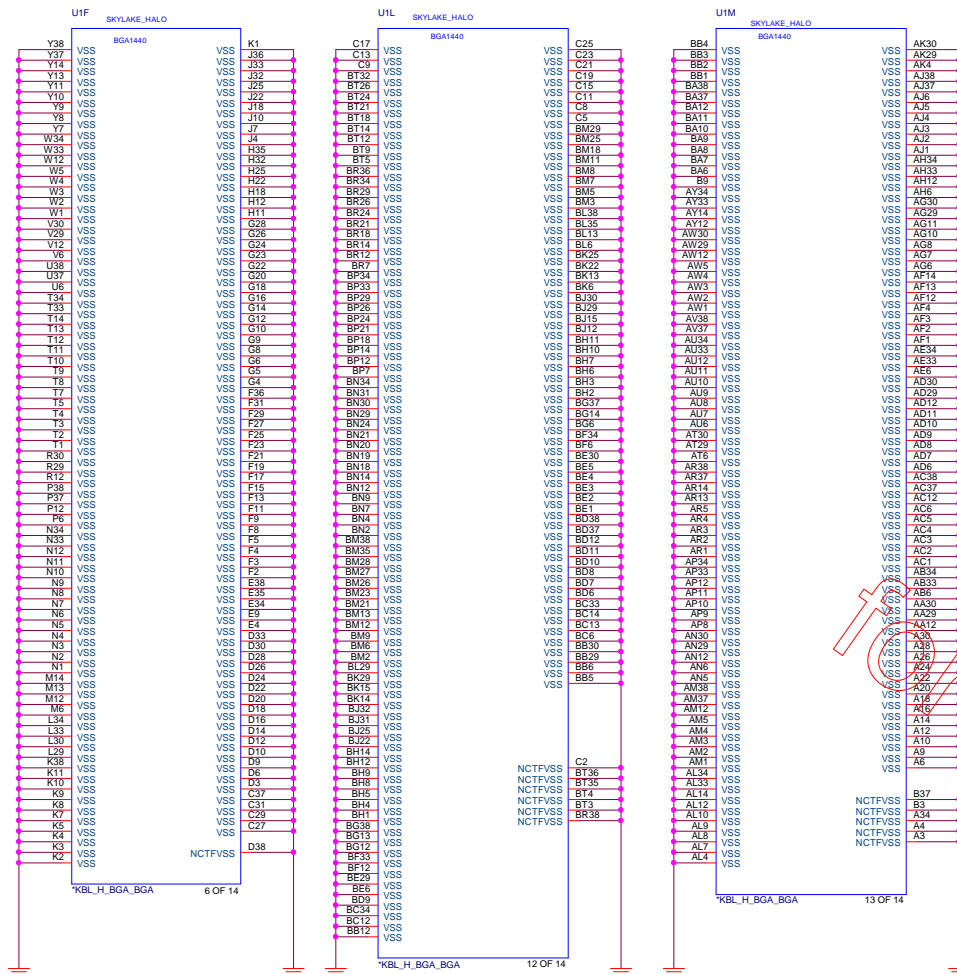


**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

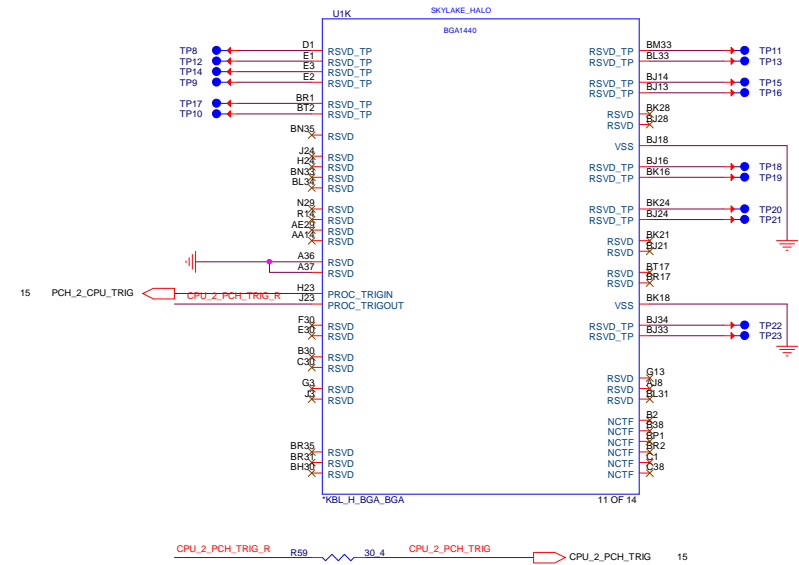
| Size                              | Document Number          | Rev           |
|-----------------------------------|--------------------------|---------------|
| Custom                            | 07 - SKL 6/7 (POWER&GND) | 1A            |
| Date: Thursday, November 10, 2016 |                          | Sheet 7 of 52 |



## KBL-HProcessor (GND)



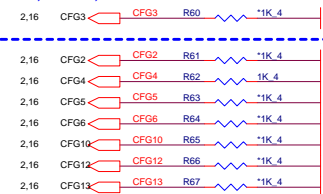
## KBL-H Processor (RESERVED, CFG)



## Processor Strapping

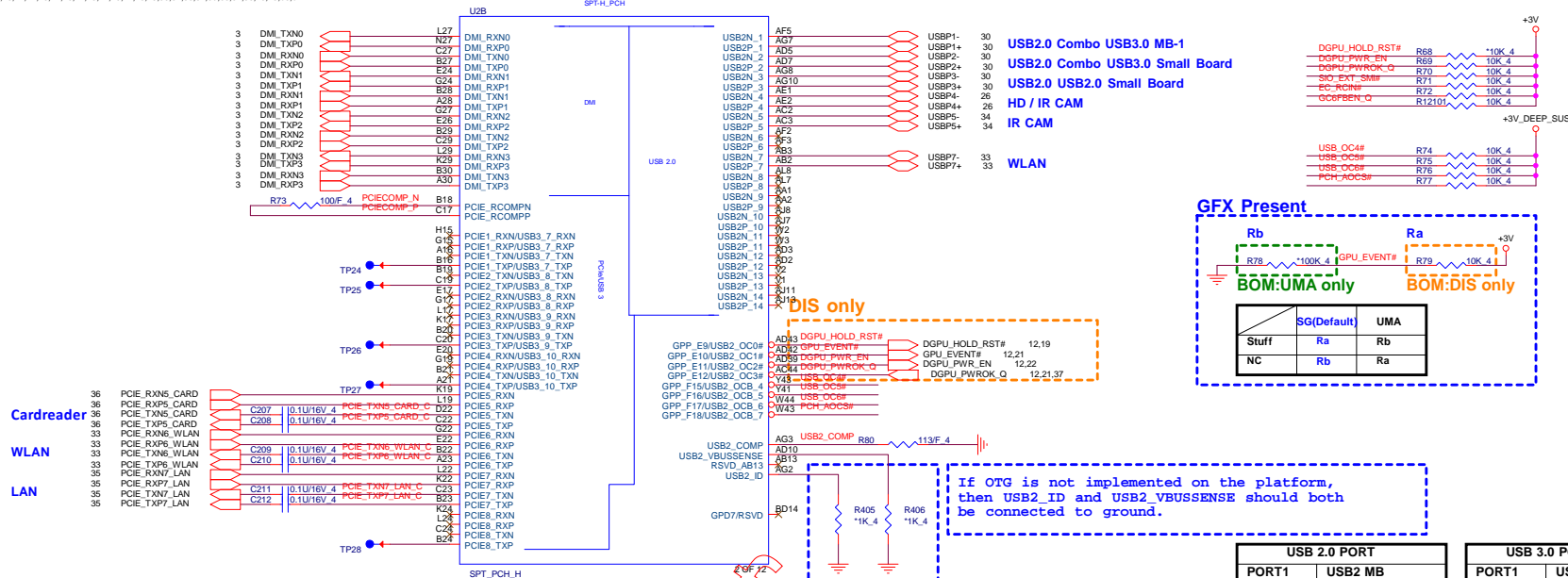
The CFG signals have a default value of '1' if not terminated on the board

0 Enable; SET DFX ENABLED BIT IN DEBUG  
1 , Disable;





+3V DEEP\_SUS 10,12,13,14,16,18  
+3V 5,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51



**GFX Present**

BOM:UMA only BOM:DIS only

|       | SG(Default) | UMA |
|-------|-------------|-----|
| Stuff | Ra          | Rb  |
| NC    | Rb          | Ra  |

**DIS only**

AD13 DGPU\_HOLD\_RST#  
AD12 DGPU\_EVENT#  
AD10 DGPU\_PWROK\_Q  
AD11 DGPU\_PWROK\_Q  
W43 USB\_OC4#  
W44 USB\_OC5#  
W43 PCH\_XOC5#

If OTG is not implemented on the platform, then USB2\_ID and USB2\_VBUSSENSE should both be connected to ground.

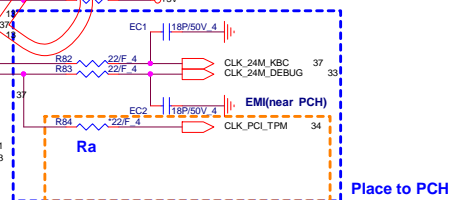
| USB 2.0 PORT |                     |
|--------------|---------------------|
| PORT1        | USB2 MB             |
| PORT2        | USB2 DB             |
| PORT3        | USB2 DB             |
| PORT4        | HD /IR CAM (OPTION) |
| PORT5        | IR CAM (OPTION)     |
| PORT6        | NC                  |
| PORT7        | WLAN                |
| PORT8        | NC                  |
| PORT9-14     | NC                  |

| USB 3.0 PORT |           |
|--------------|-----------|
| PORT1        | USB3 MB   |
| PORT2        | USB3 DB   |
| PORT3        | NC        |
| PORT4        | 3D CAMERA |

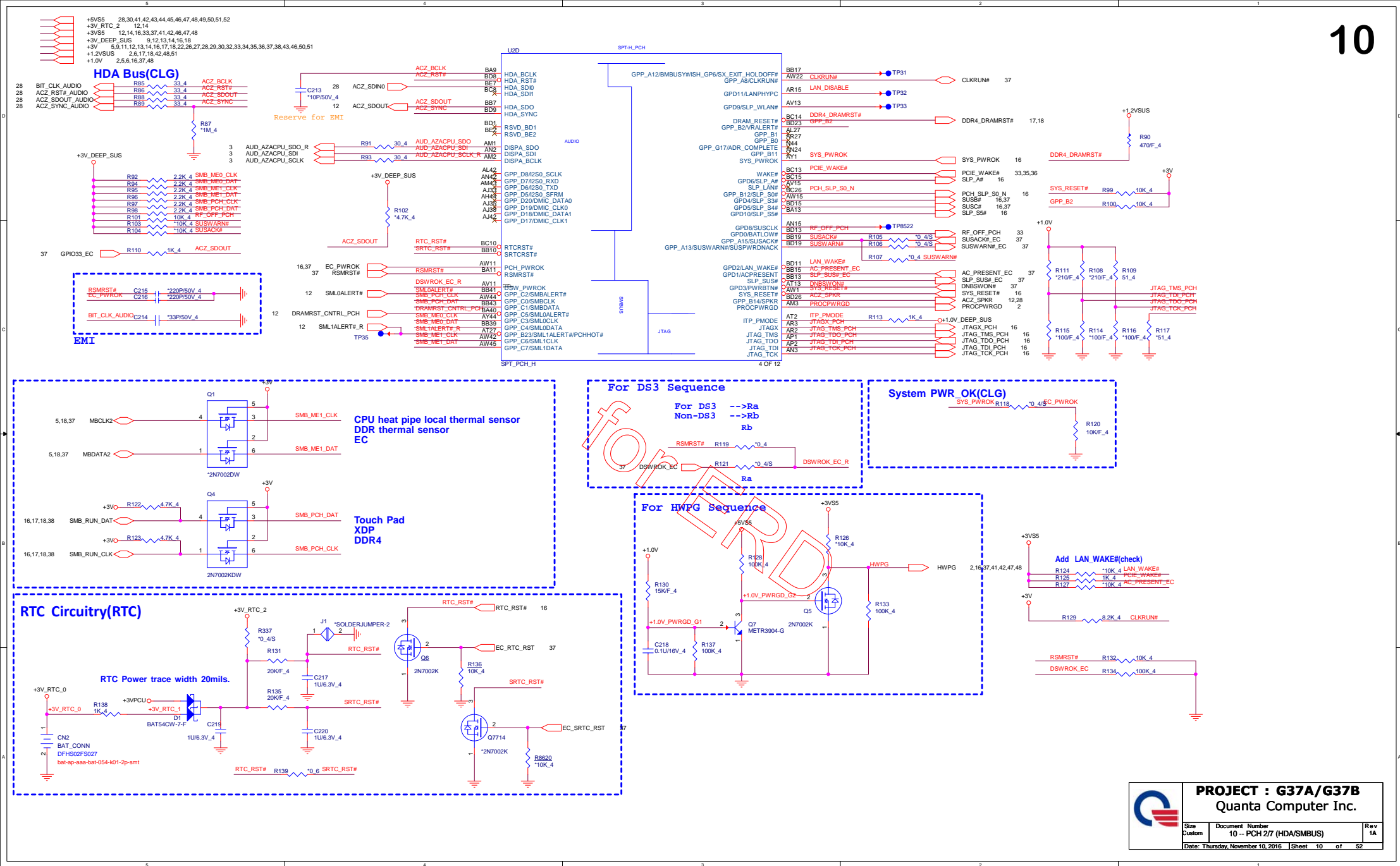
USB3.0 (M/B-1)

USB3.0 (Small Board)

USB3.0 (3D Camera)



BOM: HW TPM need Ra, Rc Stuff




 +3V    5,9,10,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51  
 +1.0V\_DEEP\_SUS    10,14,16,47,48

| HSIO MUX PORT |              |
|---------------|--------------|
| PCIE1-4       | NC           |
| PCIE5         | Cardreader   |
| PCIE6         | Wlan         |
| PCIE7         | Lan          |
| PCIE8         | NC           |
| PCIE9/SATA0A  | SSD PCIE x 4 |
| PCIE10        |              |
| PCIE11        |              |
| PCIE12        |              |
| PCIE13        | NC           |
| PCIE14        | HDD-1        |
| PCIE15        | HDD-2        |
| PCIE16        | ODD          |
| PCIE17        | NC           |
| PCIE18-20     | NC           |

SSD PCIE x4 LANE

**HDD-1 (SATA1B 6Gb/s)**

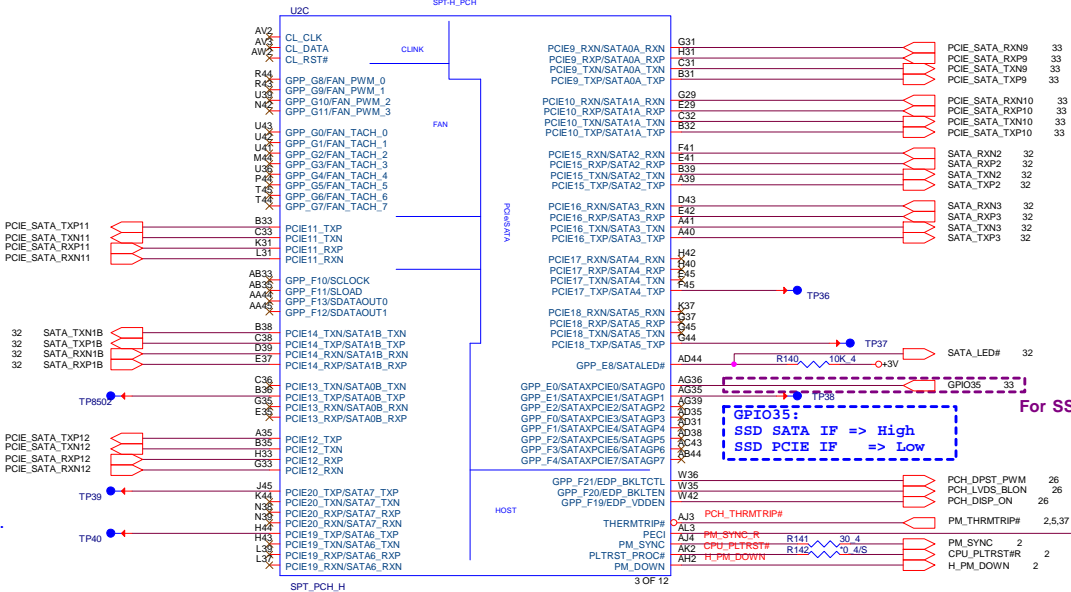
SSD PCIE x4 LANE

SSD PCIE x4 (SATA0A) LANE

SSD PCIE x4 LANE

**HDD-2 (SATA2 6Gb/s)**

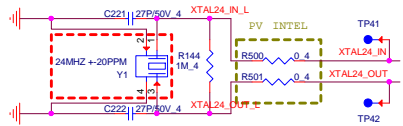
ODD (SATA3 3.0Gb/s)



For SSD Det (SATA0A)

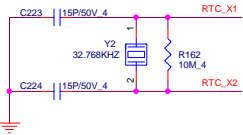
**BOM:SSD only**

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.



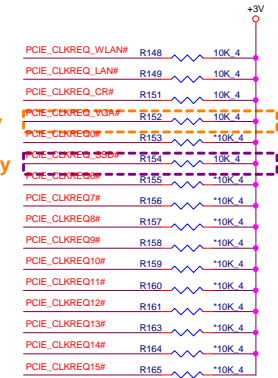
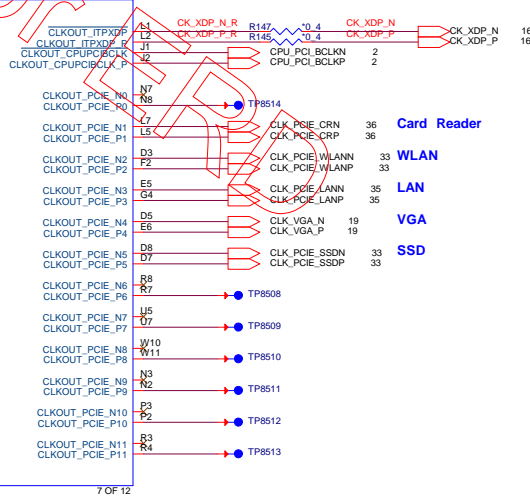
**Crystal Components with Surrounding 10 mil Wide GND Shield Trace**  
**Break Out: 4-10 mil Wide GND Shield Trace**

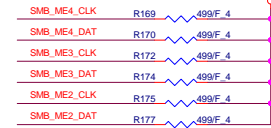
**RTC Clock 32.768KHz**



**BOM:DIS only**

**BOM:SSD only**

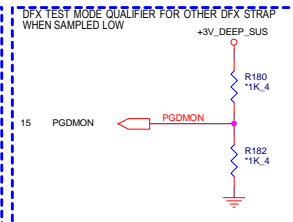




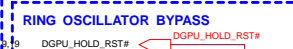
## PCH SPI ROM(CLG)



**HIGH:** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. (CRITICAL)



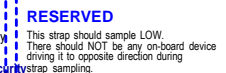
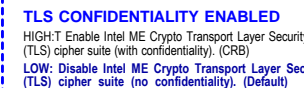
XTAL INPUT IS SINGLE ENDED IF  
SAMPLED LOW ELSE DIFFERENTIAL +3V<sub>DEEP\_SUS</sub>



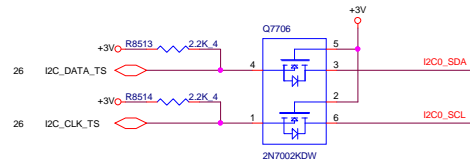
XTAL INPUT FREQUENCY[0]

9,21 GPU\_EVENT#

GPU\_EVENT#



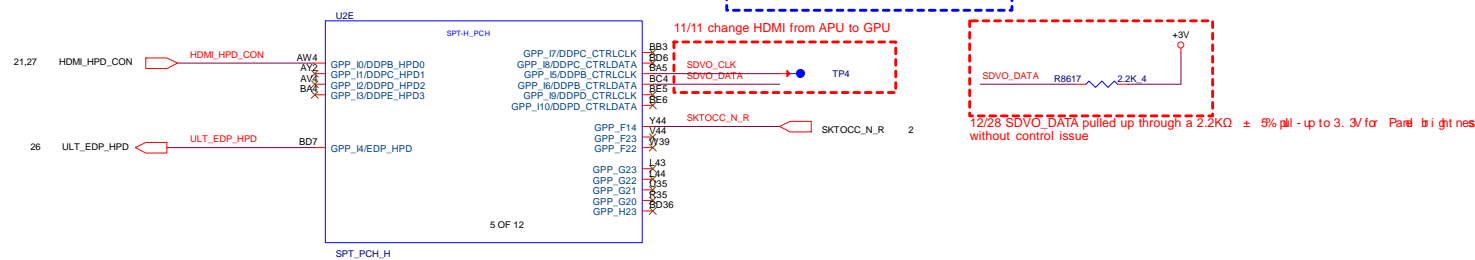
|                                   |  |                |
|-----------------------------------|--|----------------|
| Size<br>Custom                    | Document Number<br>12 -- PCH 4/7 (GPIO/MISC) | Rev<br>1A      |
| Date: Thursday, November 10, 2016 |  | Sheet 12 of 52 |



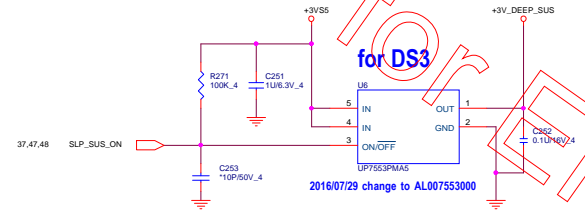
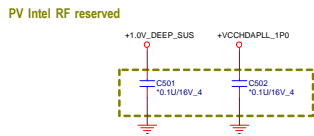
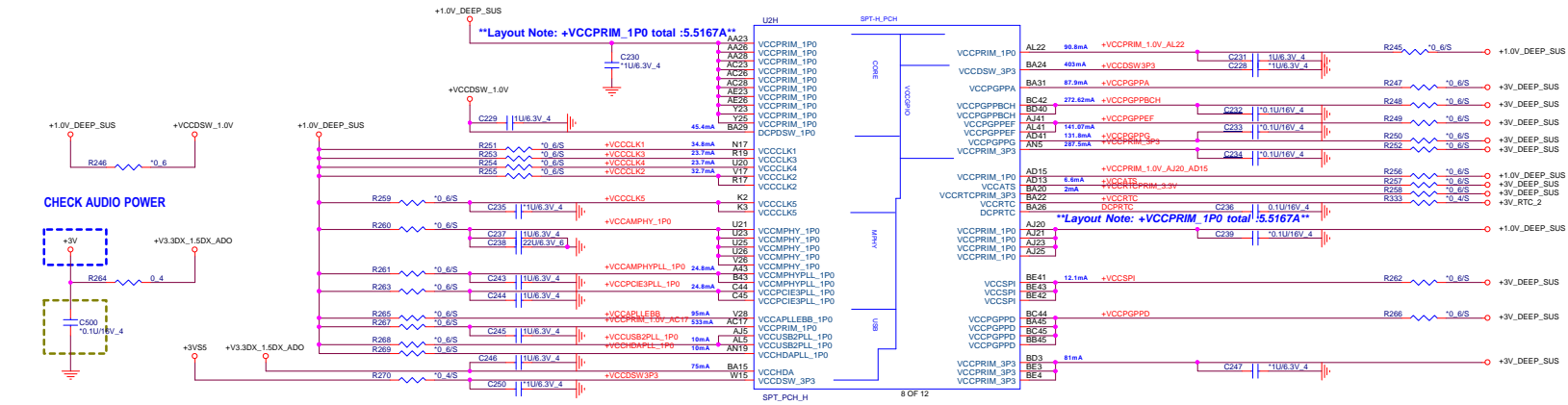
| Model      | BOARD_ID[8:7]<br>ID8;ID7   | BOARD_ID[6:5]<br>ID6;ID5 | Board ID [4:3]<br>ID4;ID3 | BOARD_ID[2:1]<br>ID2;ID1  | BOARD_ID[0]<br>ID0   |
|------------|----------------------------|--------------------------|---------------------------|---|----------------------|
| Definition | 00 Non 3D CAM<br>01 3D CAM | 00 Reserved              | Reserved                  | 00 15" P SKL H<br>01 17" P SKL H<br>10 17" SP SKL H<br>11 17" KBL H | 0 : U M A<br>1 : D S |

This signal has a weak internal pull-down

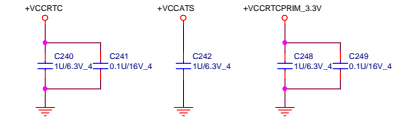
- 0 = Port C and D is not detected.
- 1 = Port C and D is detected.



+3V\_RTC\_2 10,12  
+3VSS 10,12,16,33,37,41,42,46,47,48  
+3V\_DEEP\_SUS 9,10,12,13,16,18  
+3V 5,8,10,11,12,13,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51  
+1.0V\_DEEP\_SUS 10,11,16,47,48



20mils

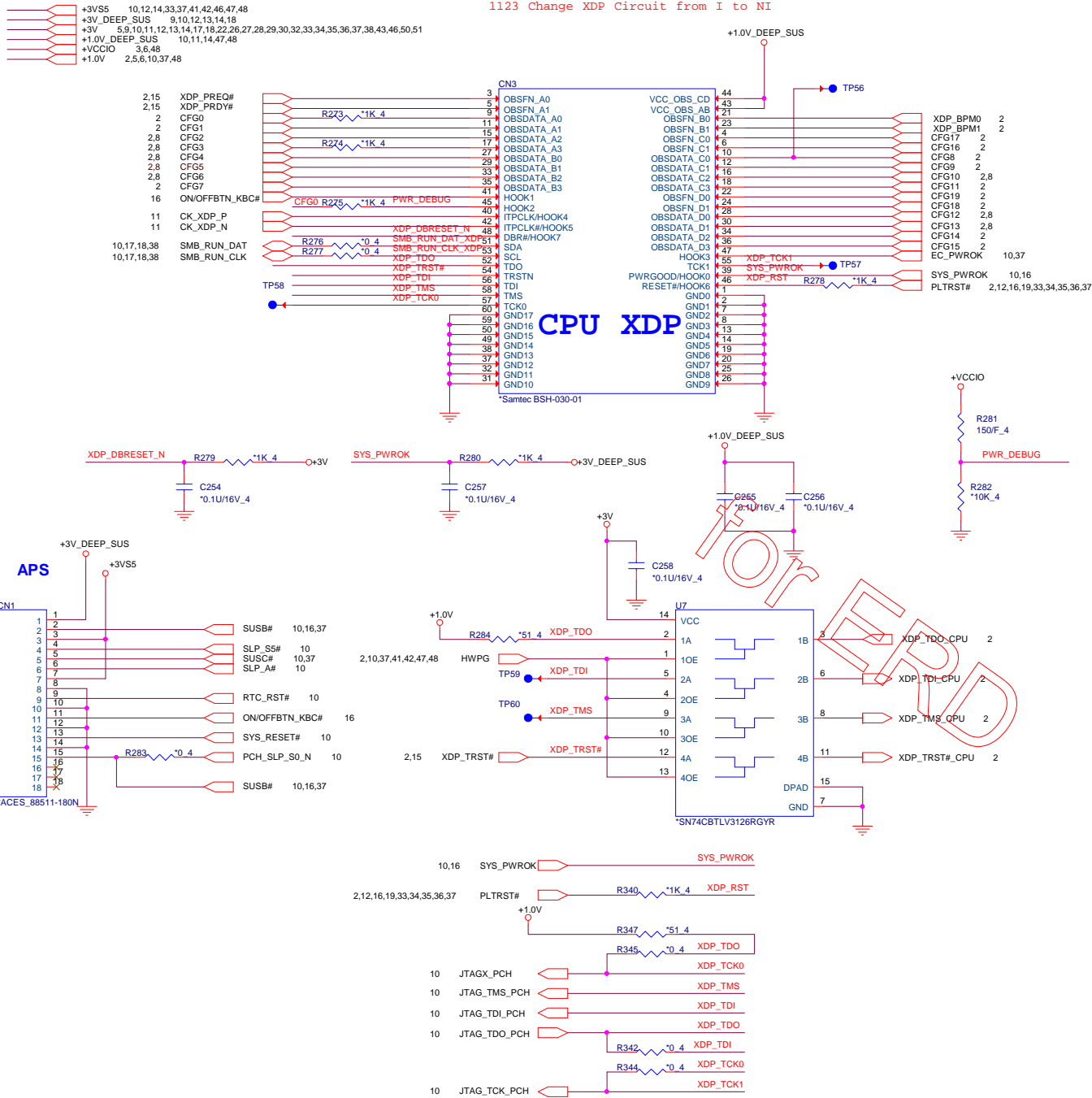


|  |                       |  |     |
|--|-----------------------|--|-----|
|  |                       |  |     |
| PROJECT : G37A/G37B                                |                       |  |     |
| Quanta Computer Inc.                               |                       |  |     |
| Size   | Document Number       |  | Rev |
| Custom   | 14 -- PCH 6/7 (POWER) |  | 1A  |
| Date: Thursday, November 10, 2016   Sheet 14 of 62 |                       |  |     |

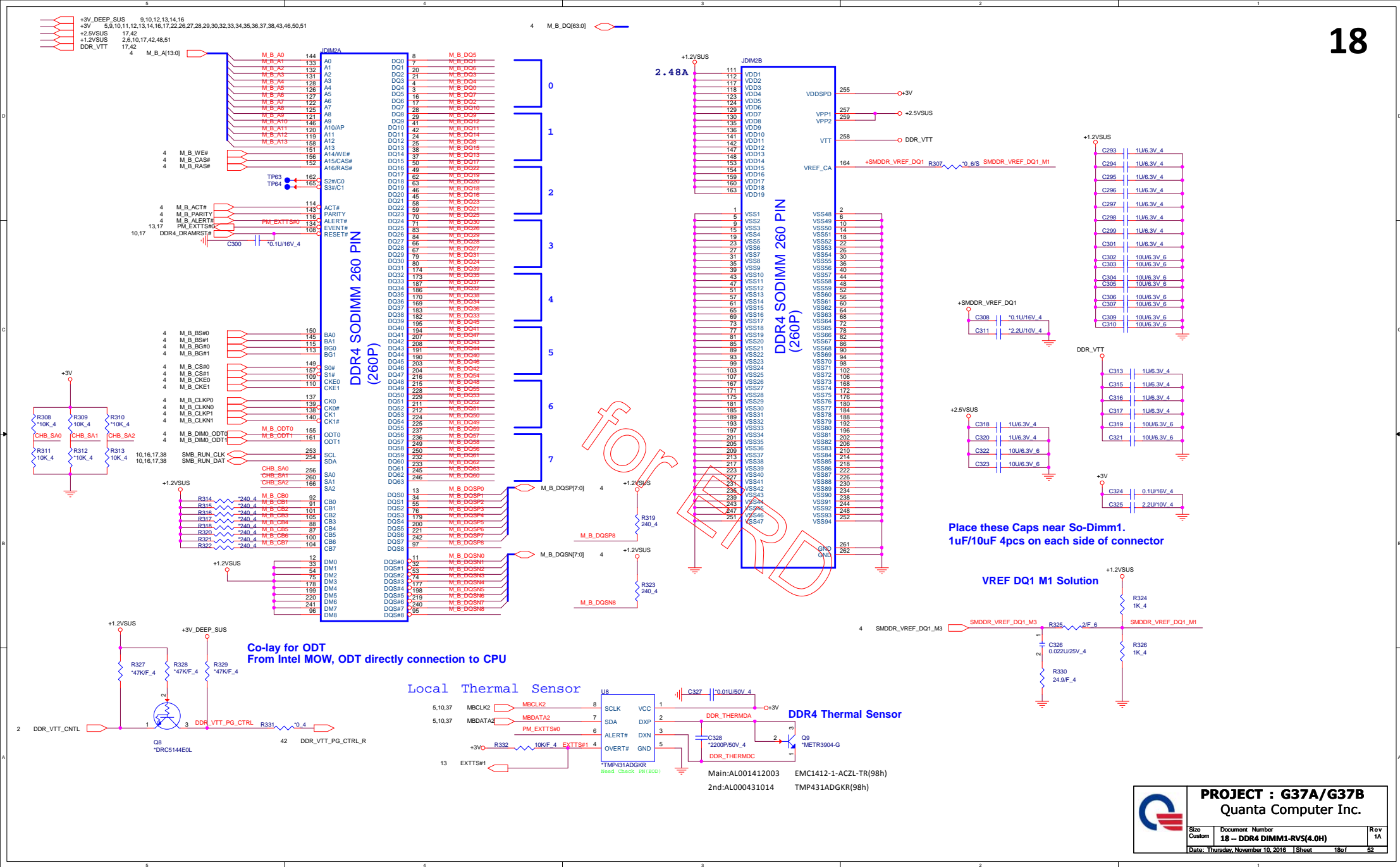


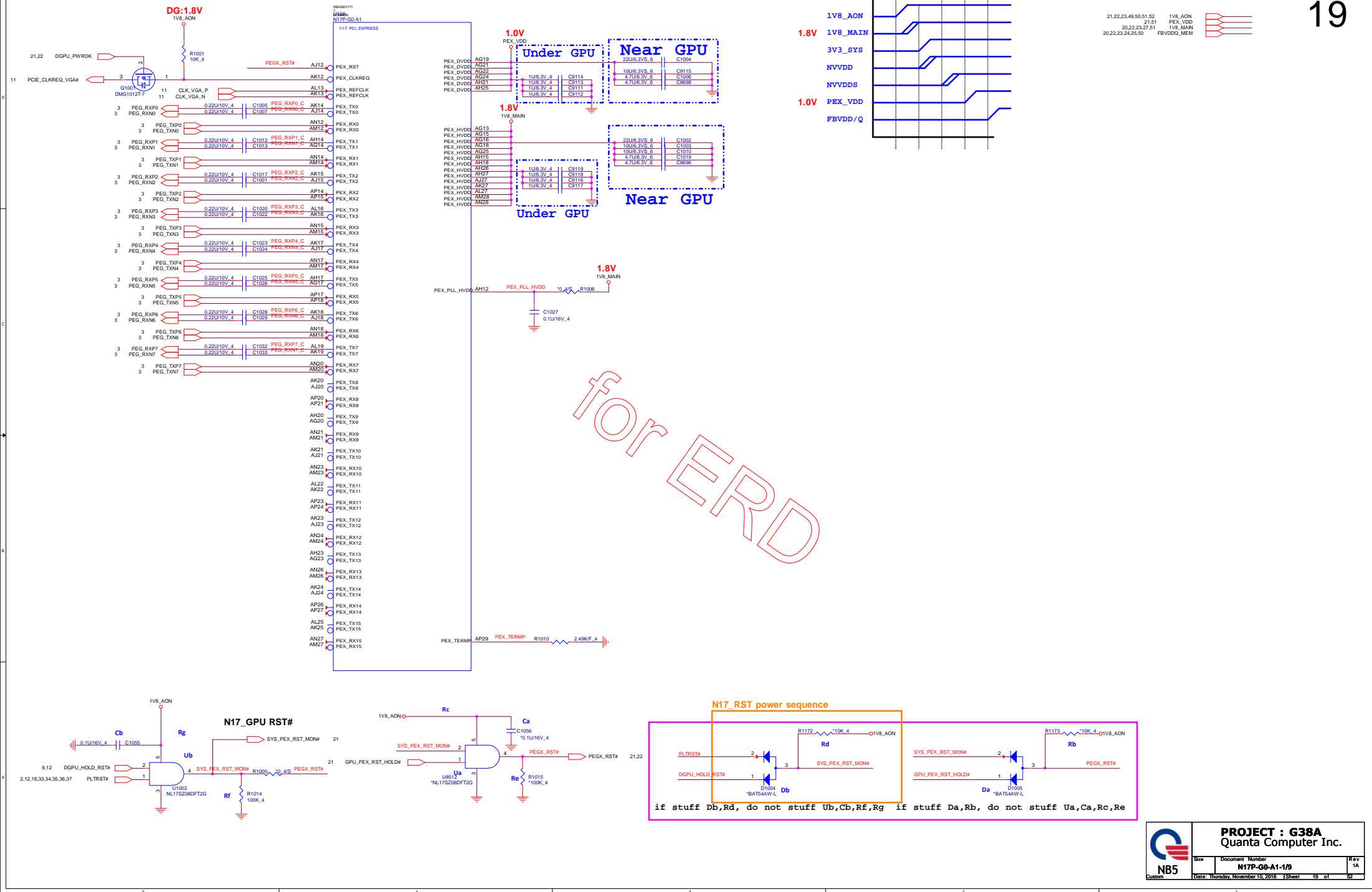


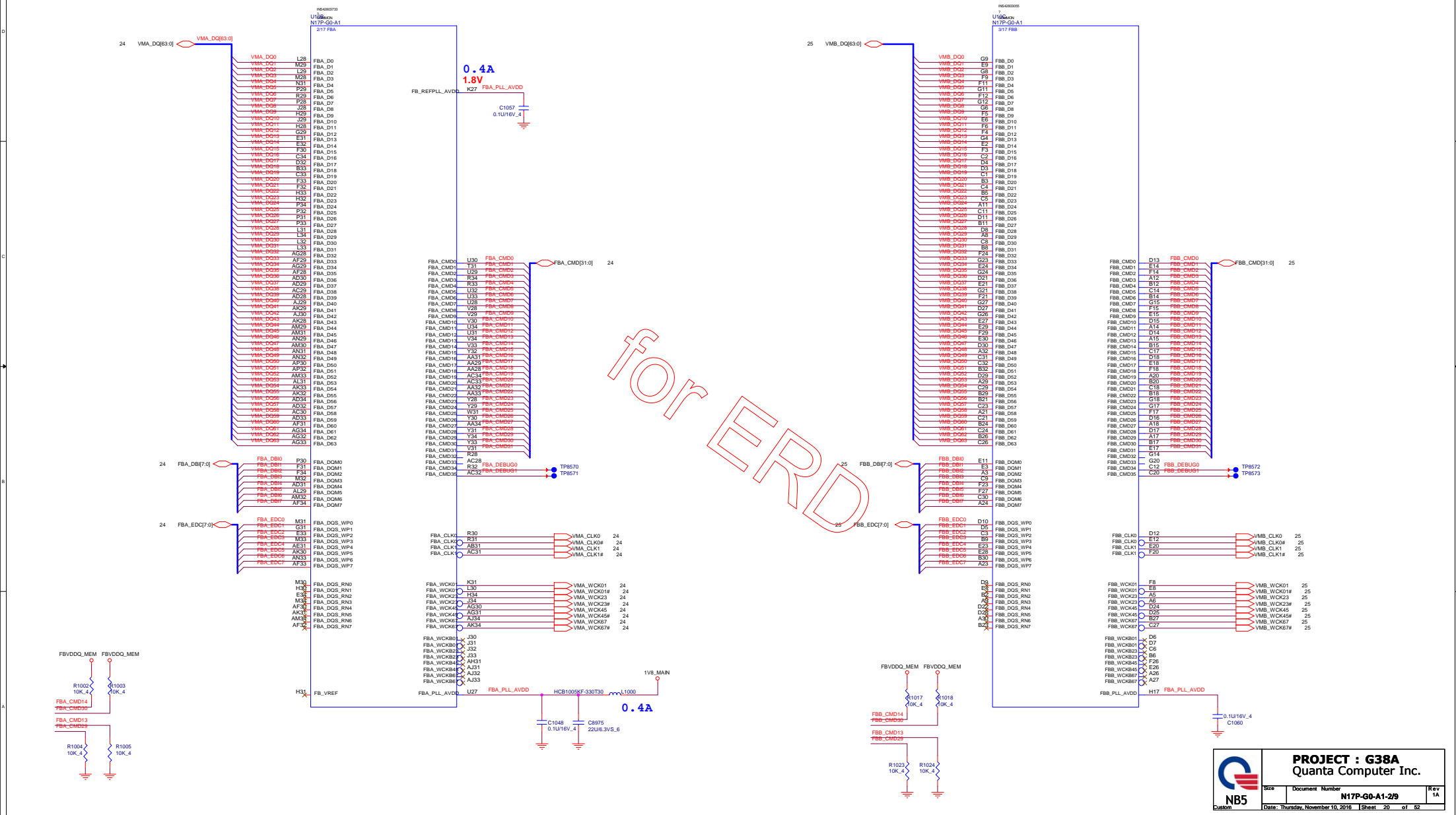
1123 Change XDP Circuit from I to NI

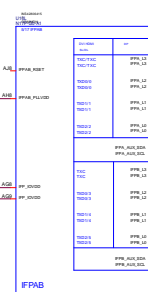








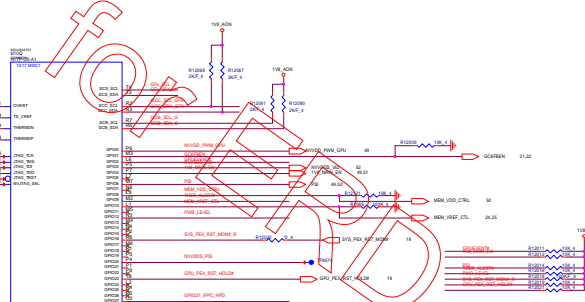
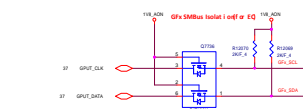




STRAP[2:0] VRAM Table for N17P-G0 GDDR5 Recommended Memories

| STRAP[2:0] | DESCRIPTION         | Vendor        | Vendor PN          | TOP P/N     | OS P/N      | Default |
|------------|---------------------|---------------|--------------------|-------------|-------------|---------|
| Str0       | GDDR5 256Mx32 7 GHz | SamSung E die | K4D513258F-1028    | AKGSG00T160 | AKGSG00T168 |         |
| Str1       | GDDR5 256Mx32 7 GHz | Metrix A die  | M512358F32P-701A   | AKGSG00T167 | AKGSG00T166 |         |
| Str2       | GDDR5 256Mx32 7 GHz | Hynix A die   | H5GQ8324A28-B0C    |             |             |         |
| Str3       | GDDR5 128Mx32 7 GHz | SamSung E die | K4D413258F-1028    | AKGSG00T161 | AKGSG00T162 |         |
| Str4       | GDDR5 128Mx32 7 GHz | Metrix A die  | K2M41328ABP-70-P-B | AKGSPW0T168 | AKGSPW0T167 |         |
| Str5       | GDDR5 128Mx32 7 GHz | Hynix A die   | H5GQ4824A28-B0C    | AKGSPW0T166 | AKGSPW0T165 |         |

| Vendor | Size          | PN                     |
|--------|---------------|------------------------|
| NTE-DX | W80000        | AKSEZN000 (W2004PWS00) |
| NTE-DY | 8 Giga device | 1Mb                    |



Throttle

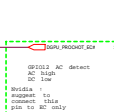


Table 14.2 GPIO Descriptions for GB4C-128 Packages

| GPIO Number | GPIO Name       | I/O | Functional Description                       | I/O Termination                                   |
|-------------|-----------------|-----|--|---|
| GPIO0       | HWPGD_PWN_VID   | O   | Pin0 Output to control HWPGD                 | 0 to VDD Pin output                               |
| GPIO1       | GCMAI_GCK_P8_DI | O   | Pin Enable for GCK 2.1                       | Open Source 10 kΩ pull-down                       |
| GPIO2       | GCMAI_GPU_POWER | I   | GPU power signal for GCK 2.1                 | 100 kΩ pull-up to VDD_ACH, unless driven actively |
| GPIO3       | HWPGD_STAN_PWN  | O   | Pin0 output to control the STAN power supply | 0 to VDD output                                   |
| GPIO4       | GCMAI_HL_NAR_DI | O   | GPU power sequencing for GCK 2.1             | Open Drain 100 kΩ pull-up to VDD_ACH              |
| GPIO5       | PWR_LCK         | I   | Active low Frame Lock                        | Open Drain 100 kΩ pull-up to VDD_ACH              |

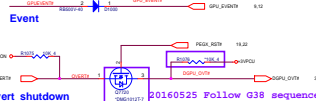
Table 14.3 GPIO Descriptions for GB4C-128 Packages (Continued)

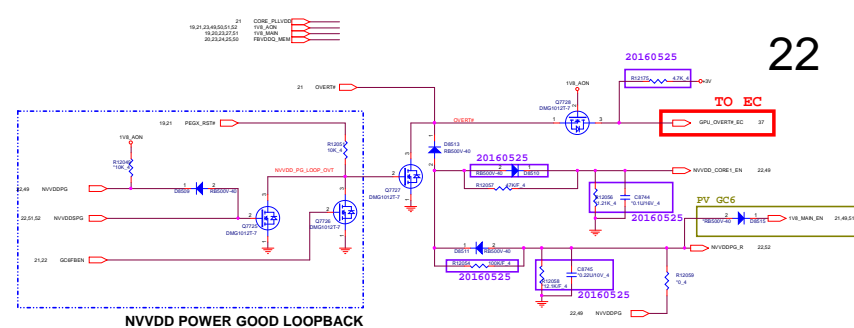
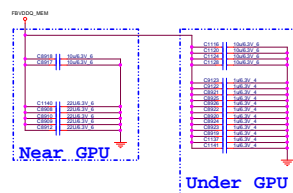
| GPIO Number | GPIO Name         | I/O | Functional Description              | I/O Termination  |
|-------------|-------------------|-----|-------------------------------------|--|
| GPIO6       | HWPGD_P8          | O   | Phase Shedding (see Section 14.3.3) | 10 kΩ pull-up to VDD_ACH to enable multiple phases             |
| GPIO7       | LED_BL_PWN        | O   | Panel Backlight enable              | 100 kΩ pull-down   |
| GPIO8       | MEM_VDD_CTL       | O   | Memory voltage control              | Pin up/pull-up to VDD to set the VDD_ACH power mode to VDD_ACH |
| GPIO9       | THRM_ALERT        | I/O | Active Low Thermal Alert            | Open Drain 100 kΩ pull-up to VDD_ACH                           |
| GPIO10      | MEM_VREF_CTL      | O   | Memory VREF Control                 | 100 kΩ pull-down   |
| GPIO11      | LED_VDD           | O   | Quadro Power enable                 | 100 kΩ pull-down   |
| GPIO12      | PWR_LEVEL         | I   | Power supply detect input           | 100 kΩ pull-up to VDD_ACH                                      |
| GPIO13      | LED_BLEND         | O   | LED Backlight Enable                | Panel Backlight Enable   |
| GPIO14      | HPD_PPFA          | I   | Hot Plug Detect for HPFA            | Inverted input. See Figure 14.3                                |
| GPIO15      | HPD_PPFB          | I   | Hot Plug Detect for HPFB            | Inverted input. See Figure 14.3                                |
| GPIO16      | GCMAI_PCH_RST_ACH | O   | System side PCIe reset monitor      | 10 kΩ pull-up to VDD_ACH unless actively driven                |
| GPIO17      | HPD_PPFD          | I   | Hot Plug Detect for HPFD            | Inverted input. See Figure 14.3                                |
| GPIO18      | HPD_PPFE          | I   | Hot Plug Detect for HPFE            | Inverted input. See Figure 14.3                                |
| GPIO19      | SD_VIDEN          | O   | SD Video I/O Signal                 | 100 kΩ pull-down   |
| GPIO20      | FW_LOAD           | I/O |                                     |  |
| GPIO21      | FW_LOAD           | I/O |                                     |  |
| GPIO22      | FW_LOAD           | I/O |                                     |  |

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

| GPIO Number | GPIO Name            | I/O | Functional Description      | I/O Termination                     |
|-------------|----------------------|-----|-----------------------------|-------------------------------------|
| GPIO23      | GCMAI_GPU_RESET_HOLD | O   | GPU PCIe self-reset control | Open Drain 10 kΩ pull-up to VDD_ACH |
| GPIO24      | HPD_PPFF             | I   | Hot plug detect for HPFF    | Inverted input. See Figure 14.3     |
| GPIO25      | UNLCKED              | O   |                             |                                     |
| GPIO26      | UNLCKED              | O   |                             |                                     |
| GPIO27      | HPD_PPFG             | I   | Hot plug detect for HPFG    | Inverted input. See Figure 14.3     |

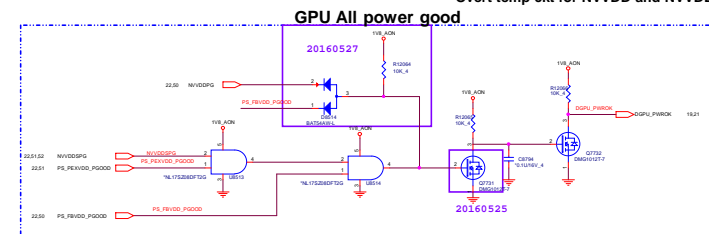
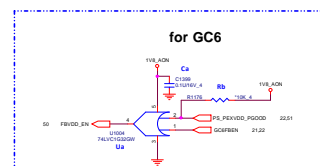
| GPIO Number | GPIO Name | I/O | Functional Description        | I/O Termination           |
|-------------|-----------|-----|-------------------------------|---------------------------|
| GPIO28      | GPIO28    | I/O | Catastrophic Over Temperature | 100 kΩ pull-up to VDD_ACH |



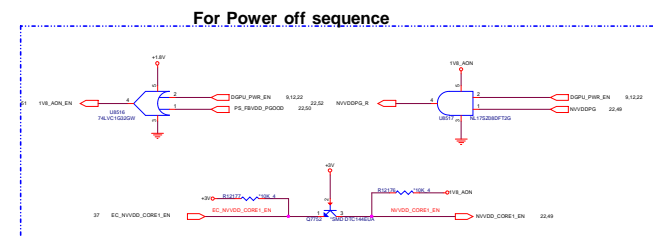


NVVDD POWER GOOD LOOPBACK

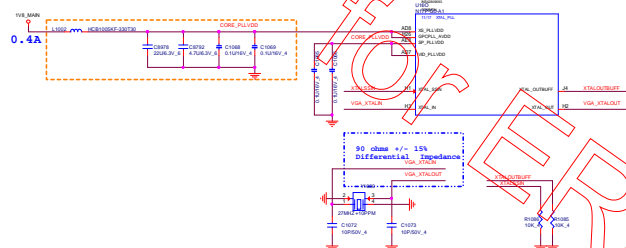
### Overt temp ckt for NVVDD and NVVDDS



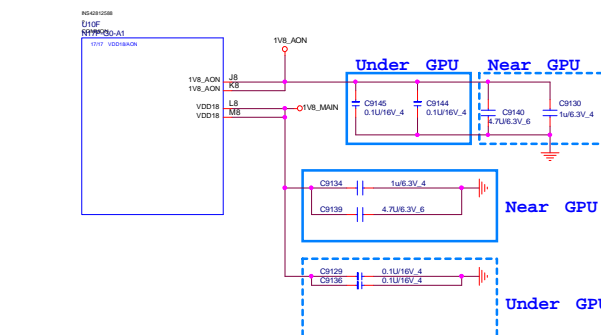
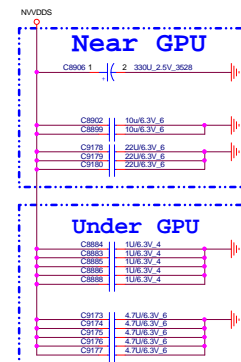
**GPU All power good**



**For Power off sequence**



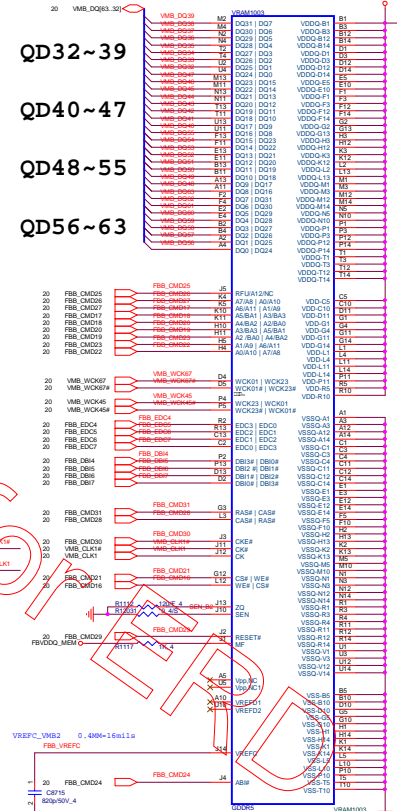






Channel 1  
<32-63>

MF=1 mirrored

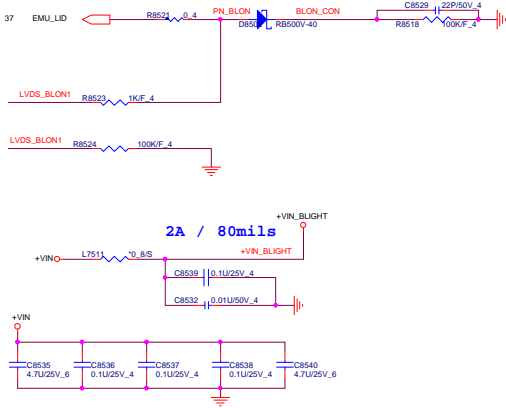


| Command Ball on GPU          |                               | DRAM Signal Definition |
|------------------------------|-------------------------------|------------------------|
| For DRAM(s) tied to DQ[31:0] | For DRAM(s) tied to DQ[63:32] |                        |
| FBA_CMD0                     | FBA_CMD16                     | CS*                    |
| FBA_CMD1                     | FBA_CMD17                     | A3_BA3                 |
| FBA_CMD2                     | FBA_CMD18                     | A2_BA0                 |
| FBA_CMD3                     | FBA_CMD19                     | A4_BA2                 |
| FBA_CMD4                     | FBA_CMD20                     | A5_BA1                 |
| FBA_CMD5                     | FBA_CMD21                     | WE*                    |
| FBA_CMD6                     | FBA_CMD22                     | A7_A8                  |
| FBA_CMD7                     | FBA_CMD23                     | A6_A11                 |
| FBA_CMD8                     | FBA_CMD24                     | AB1*                   |
| FBA_CMD9                     | FBA_CMD25                     | A12_RFU                |
| FBA_CMD10                    | FBA_CMD26                     | A0_A10                 |
| FBA_CMD11                    | FBA_CMD27                     | A1_A9                  |
| FBA_CMD12                    | FBA_CMD28                     | RAS*                   |
| FBA_CMD13                    | FBA_CMD29                     | RST*                   |
| FBA_CMD14                    | FBA_CMD30                     | CKE*                   |
| FBA_CMD15                    | FBA_CMD31                     | CAS*                   |

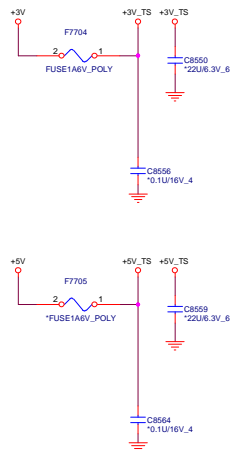
| Command Ball on GPU                | DRAM Signal Definition |
|------------------------------------|------------------------|
| FBA_CMD32 (do not connect to DRAM) | (not used)             |
| FBA_CMD33 (do not connect to DRAM) | (not used)             |
| FBA_CMD34 (do not connect to DRAM) | DEBUG0                 |
| FBA_CMD35 (do not connect to DRAM) | DEBUG1                 |

+VIN 32,38,39,40,41,42,43,44,45,46,47,48,49,50,52  
 +SVSS 10,28,30,41,42,43,44,45,46,47,48,49,50,51,52  
 +5V 27,28,29,32,38,46,49  
 +3VSS 10,12,14,16,33,37,41,42,46,47,48  
 +3V 5,9,10,11,12,13,14,16,17,18,22,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51  
 +3V\_CAM 34

# LID Switch



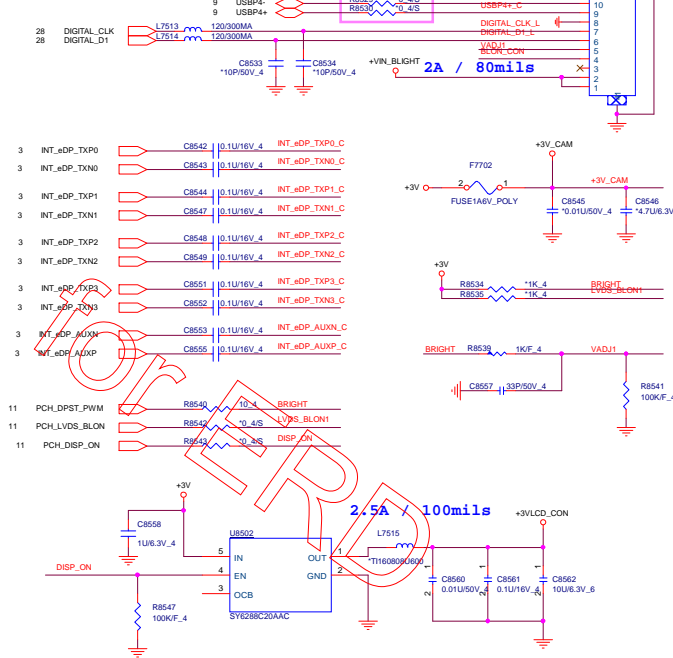
# Touch screen

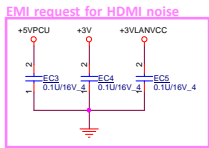


# eDP Conn.

|                 |               |
|-----------------|---------------|
| MB              | TS (VF: I2C)  |
| +3V_TS          | VDD33         |
| I2C_DATA_TS     | SDA           |
| I2C_CLK_TS      | SCL           |
| TCH_PNL_RST#_EC | EXRESETN      |
| TCH_PNL_INT#    | ATTN          |
| TS_ON           | Report_Switch |
| GND             | GND           |

# 3/9:3D CAM/HD CAM combine





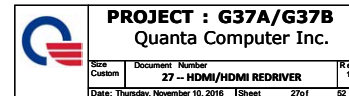
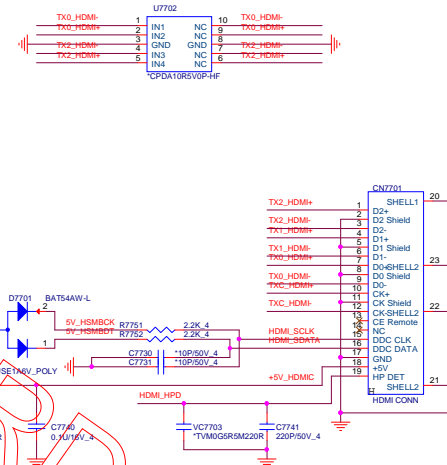
|         |       |          |          |
|---------|-------|----------|----------|
| GPU_D0  | R8626 | *120/F_4 | GPU_D0#  |
| GPU_D1  | R8627 | *120/F_4 | GPU_D1#  |
| GPU_D2  | R8628 | *120/F_4 | GPU_D2#  |
| GPU_CLK | R8629 | *120/F_4 | GPU_CLK# |

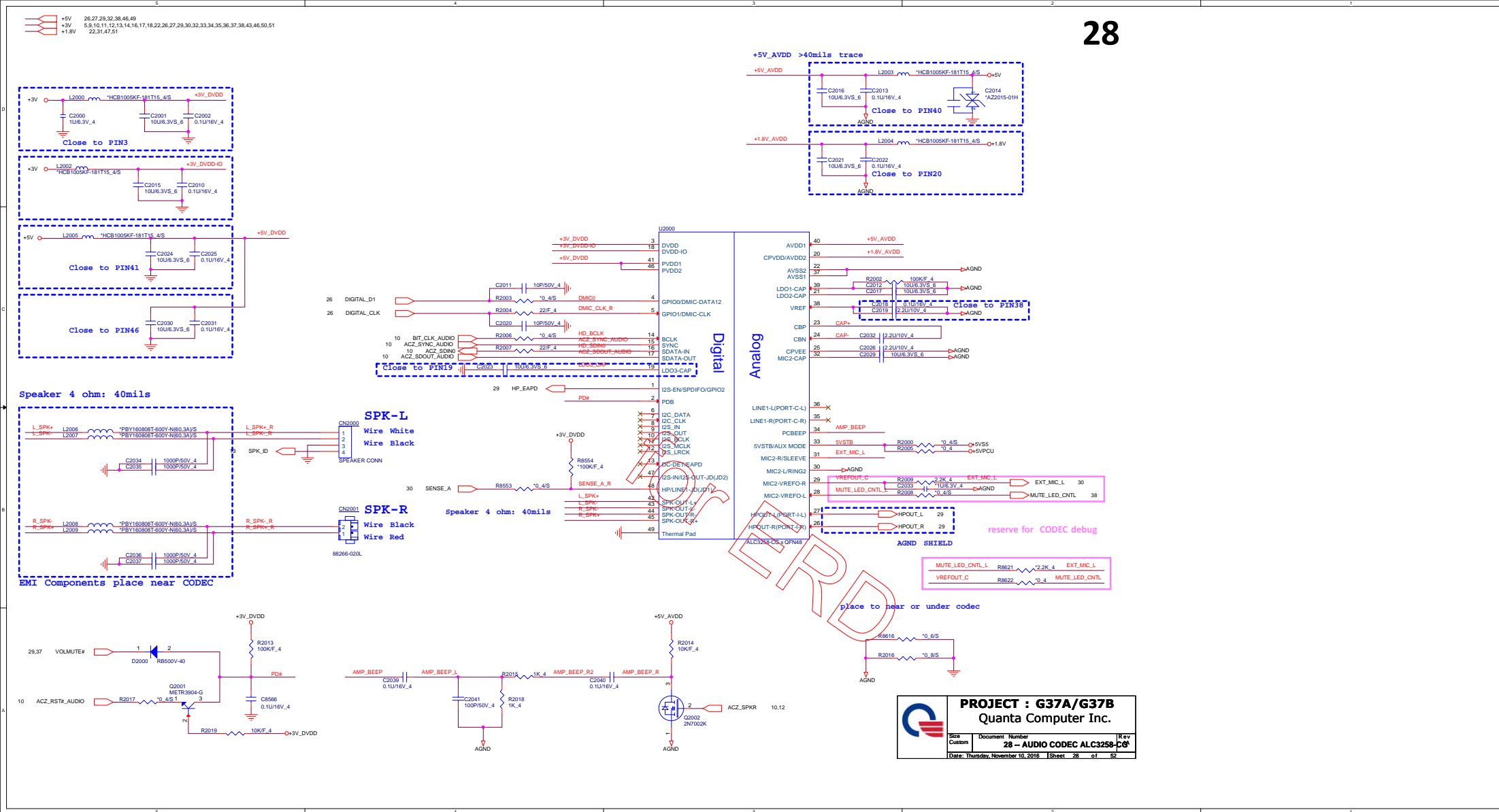
[illegible]

|           |       |         |           |
|-----------|-------|---------|-----------|
| TX2_HDMI+ | R7716 | *120F_4 | TX2_HDMI- |
| TX1_HDMI+ | R7717 | *120F_4 | TX1_HDMI- |
| TX0_HDMI+ | R7719 | *120F_4 | TX0_HDMI- |
| TXC_HDMI+ | R7722 | *120F_4 | TXC_HDMI- |

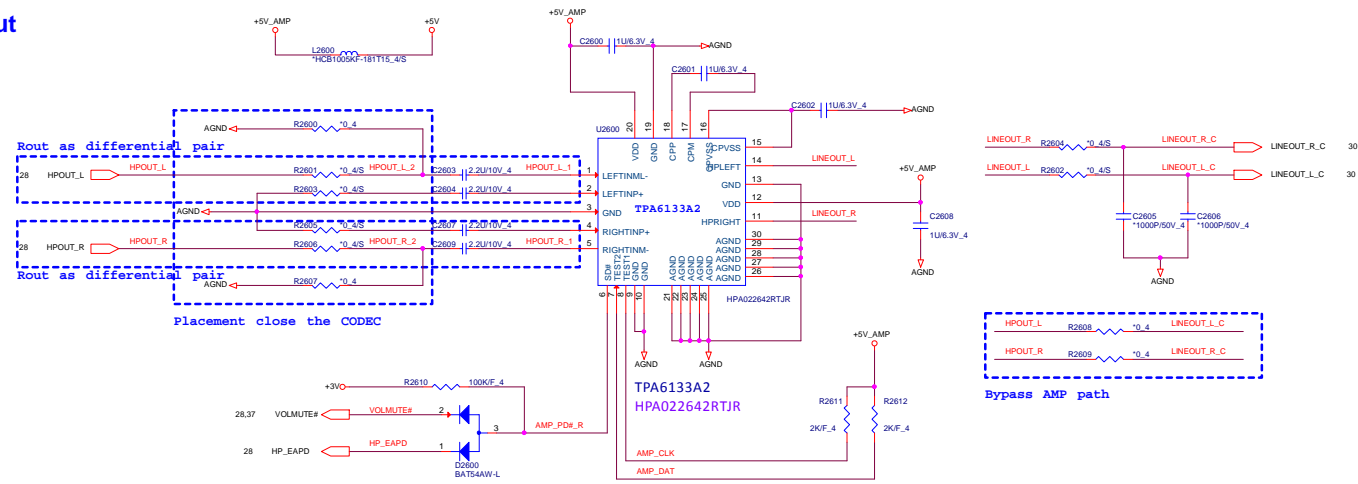
Pin connection diagram for U7701 (CPDA10R5V0P-HF). The component is a 10-pin device. The connections are as follows:


- Pin 1: TxC\_HDMI-
- Pin 2: TxC\_HDMI+
- Pin 3: TxD\_HDMI-
- Pin 4: TxD\_HDMI+
- Pin 5: GND
- Pin 6: IN4
- Pin 7: NC
- Pin 8: GND
- Pin 9: TxC\_HDMI-
- Pin 10: TxC\_HDMI+





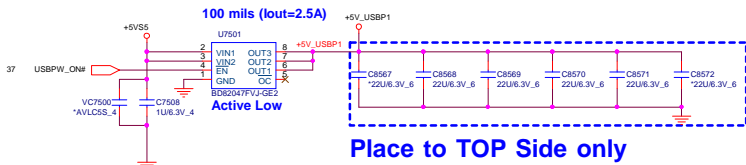
## Head Phone out



|  |  |           |
|--|--|-----------|
|  <b>PROJECT : G37A/G37B</b><br>Quanta Computer Inc. |  |           |
| Size<br>Custom   | Document Number<br><b>29- HP AMP HPA022642RTJR</b> | Rev<br>1A |
| Date: Thursday, November 10, 2016   Sheet 29 of 52   |  |           |

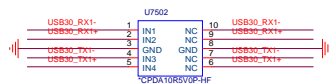
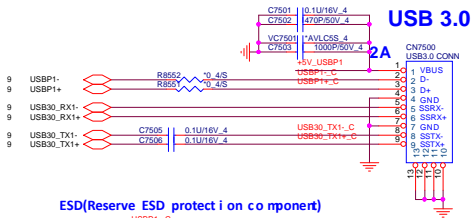


|        |   |
|--------|---|
| +5VSS  | 10,28,41,42,43,44,45,46,47,48,49,50,51,52                                   |
| +5VPCU | 5,10,21,33,37,38,40,41  |
| +3V    | 5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,32,33,34,35,36,37,38,43,46,50,51 |
| +1.8V  | 22,28,31,47,51  |



## USB 2.0/3.0 Combo

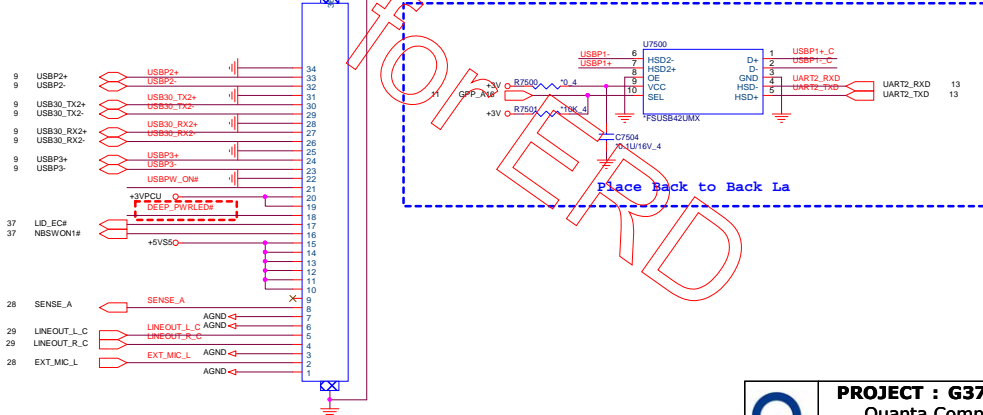
30



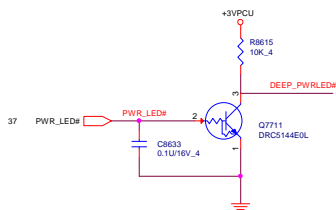
## Daughter Board

51619-03401-001  
51619-03401-001-34p1  
DFPC34FR030  
CN7702

## UART for Win7 WHQL DEBUG



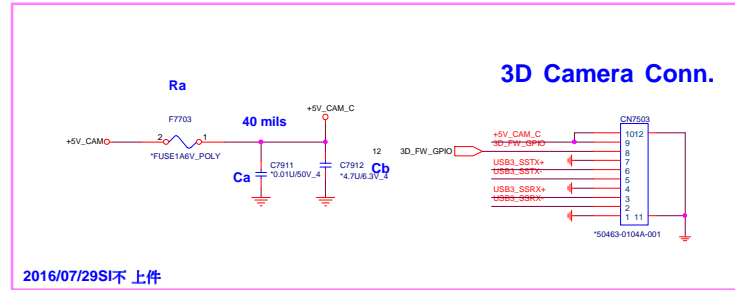
## PWR LED MOS Circuit



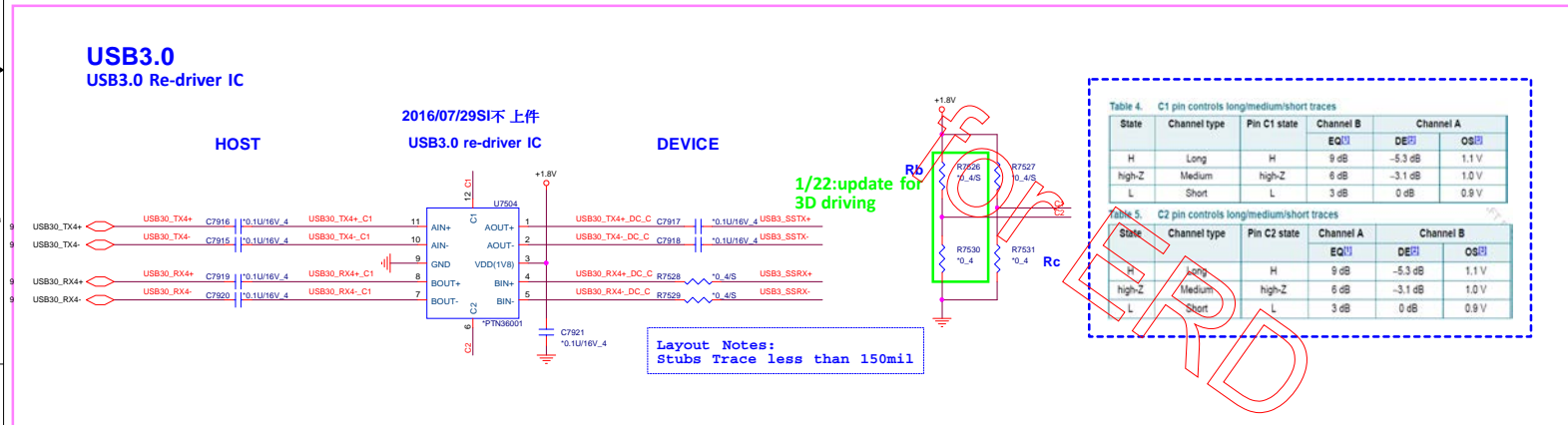
|                                   |                             |     |       |
|-----------------------------------|-----------------------------|-----|-------|
|                                   | <b>PROJECT : G37A/G37B</b>  |     |       |
|                                   | <b>Quanta Computer Inc.</b> |     |       |
| Size                              | Document Number             | Rev |       |
| Custom                            | 30 - USB3.0/DB              | 1A  |       |
| Date: Thursday, November 10, 2016 | Sheet                       | 30  | of 52 |

+5V 26,27,28,29,32,38,46,49  
+3VPCU 5,10,21,30,33,37,38,40,41  
+3V 5,8,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51  
+1.8V 22,29,47,51

BOM: 3D CAM/HD CAM combine

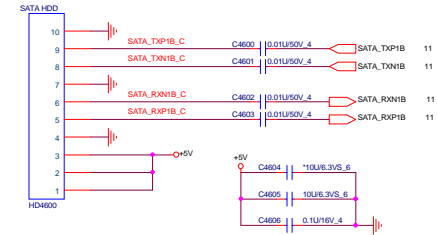


BOM: 3D CAM/HD CAM combine

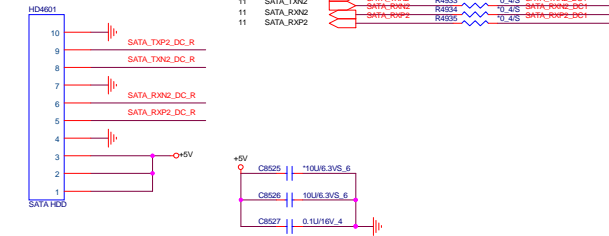


+VIN 26,38,39,40,41,42,43,44,45,46,47,48,49,50,52  
+5V 26,27,28,29,30,46,49  
+5V 6,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,33,34,35,36,37,38,43,46,50,51

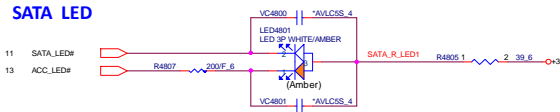
## HDD



## HDD (Close to ODD)



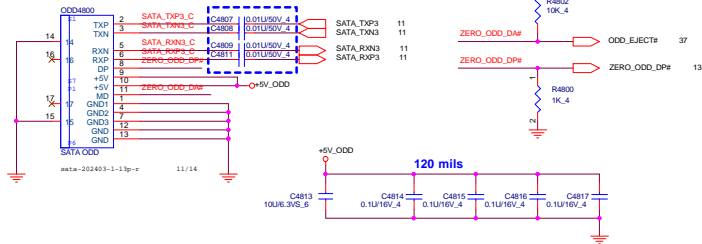
## SATA LED




|               |       |              |                |
|---------------|-------|--------------|----------------|
| SATA_TXP2_DC1 | C4624 | 0.01uF/50V_4 | SATA_TXP2_DC_R |
| SATA_TXN2_DC1 | C4625 | 0.01uF/50V_4 | SATA_TXN2_DC_R |
| SATA_RXN2_DC1 | C4626 | 0.01uF/50V_4 | SATA_RXN2_DC_R |
| SATA_RXP2_DC1 | C4627 | 0.01uF/50V_4 | SATA_RXP2_DC_R |

## SATA ODD

### Bypass CAP close CON

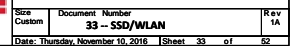


ZERO\_PWR\_ODD:  
High : ODD power down  
Low : ODD power on



**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

|                                   |                     |                |
|-----------------------------------|---------------------|----------------|
| Size                              | Document Number     | Rev            |
| Custom                            | <b>32 - HDD/ODD</b> | 1A             |
| Date: Thursday, November 10, 2016 |                     | Sheet 32 of 52 |



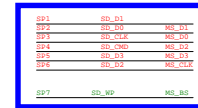




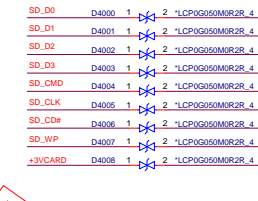
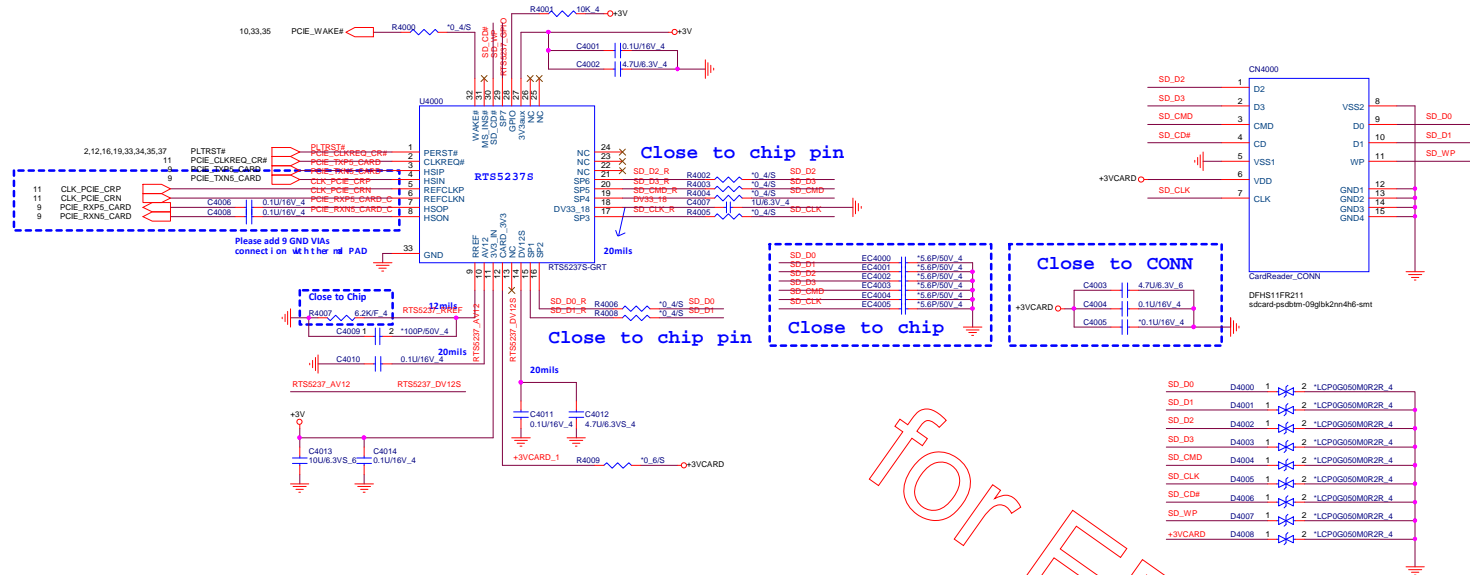
# RTS5237S PCIE CARD READER Controller


## Share Pin

SD / MMC



36

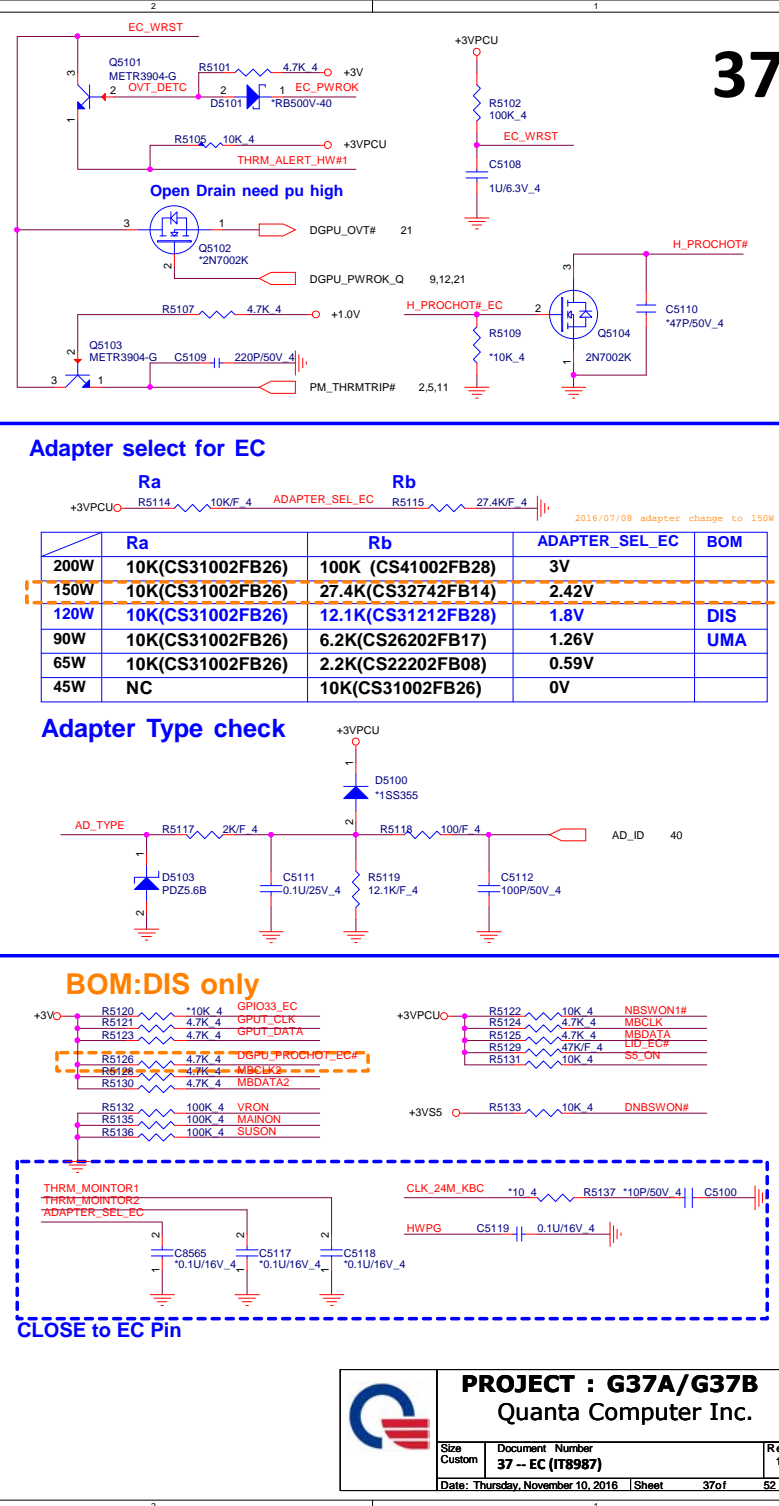
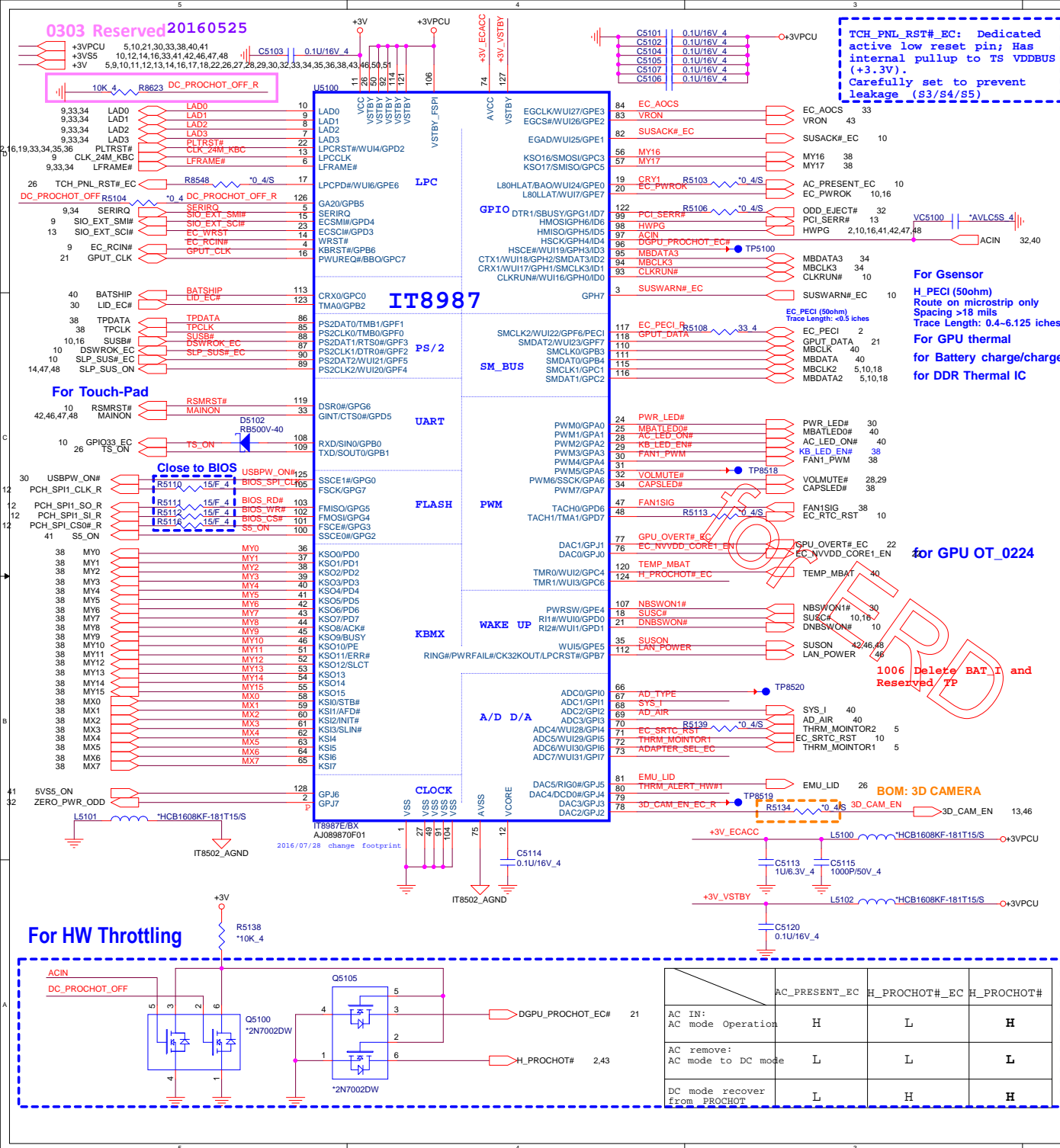


**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

| Size   | Document Number            | Rev |
|--|----------------------------|-----|
| Custom   | 36 - CR RTS5237S/CR SOCKET | 1A  |
| Date: Thursday, November 10, 2016   Sheet 36 of 52 |                            |     |

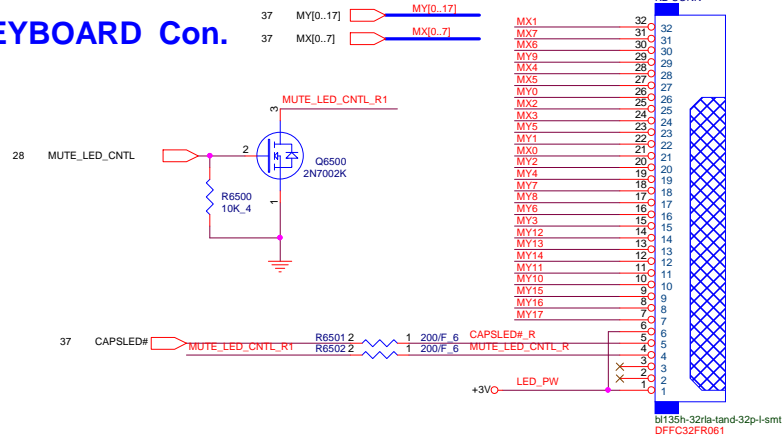


## 0303 Reserved 20160525

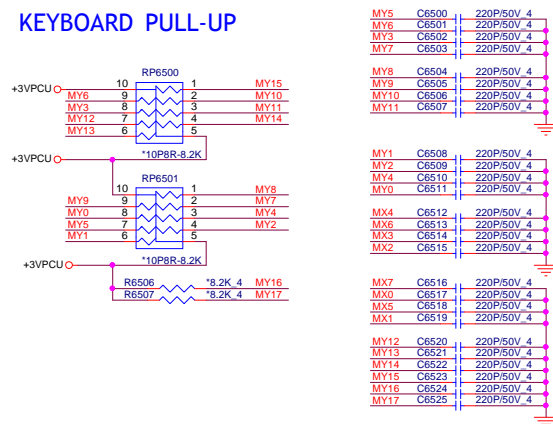


+VIN 26,32,39,40,41,42,43,44,45,46,47,48,49,50,52  
 +5V 26,27,28,29,32,46,49  
 +3VPCU 5,10,21,30,33,37,40,41  
 +3VS5 10,12,14,16,33,37,41,42,46,47,48  
 +3VSUS 46  
 +3V 5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,43,46,50,51

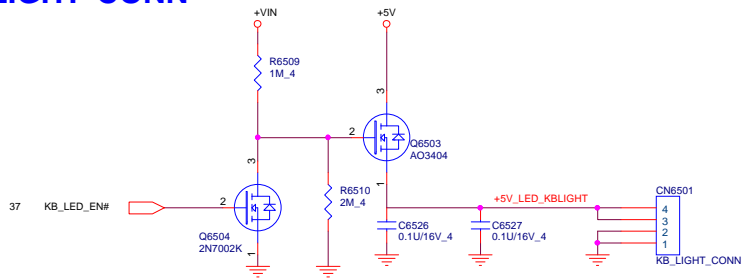
## KEYBOARD Con.



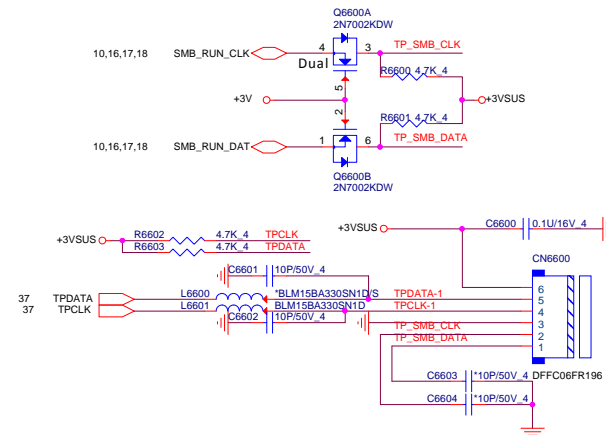
## KEYBOARD PULL-UP



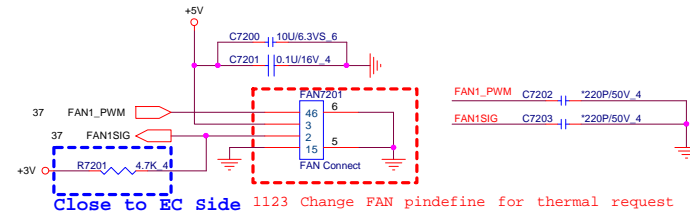
## KB LIGHT CONN



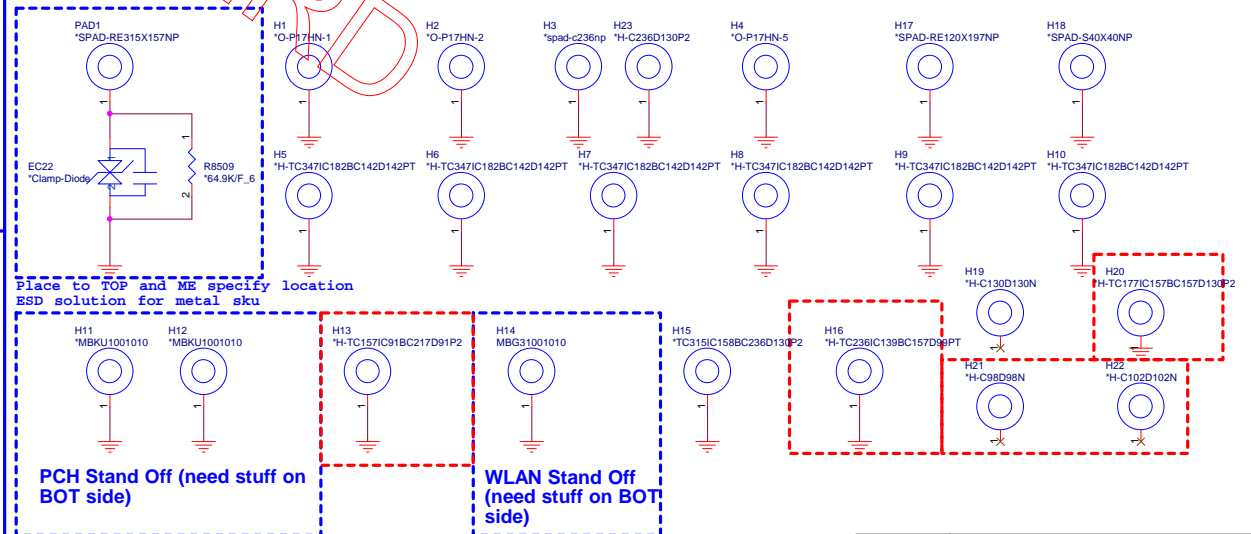
## Touch Pad Connector

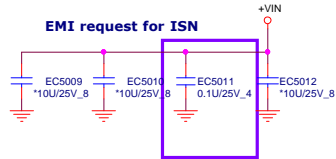
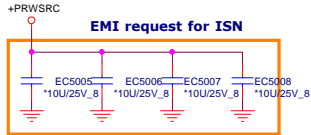


## FAN



## HOLE





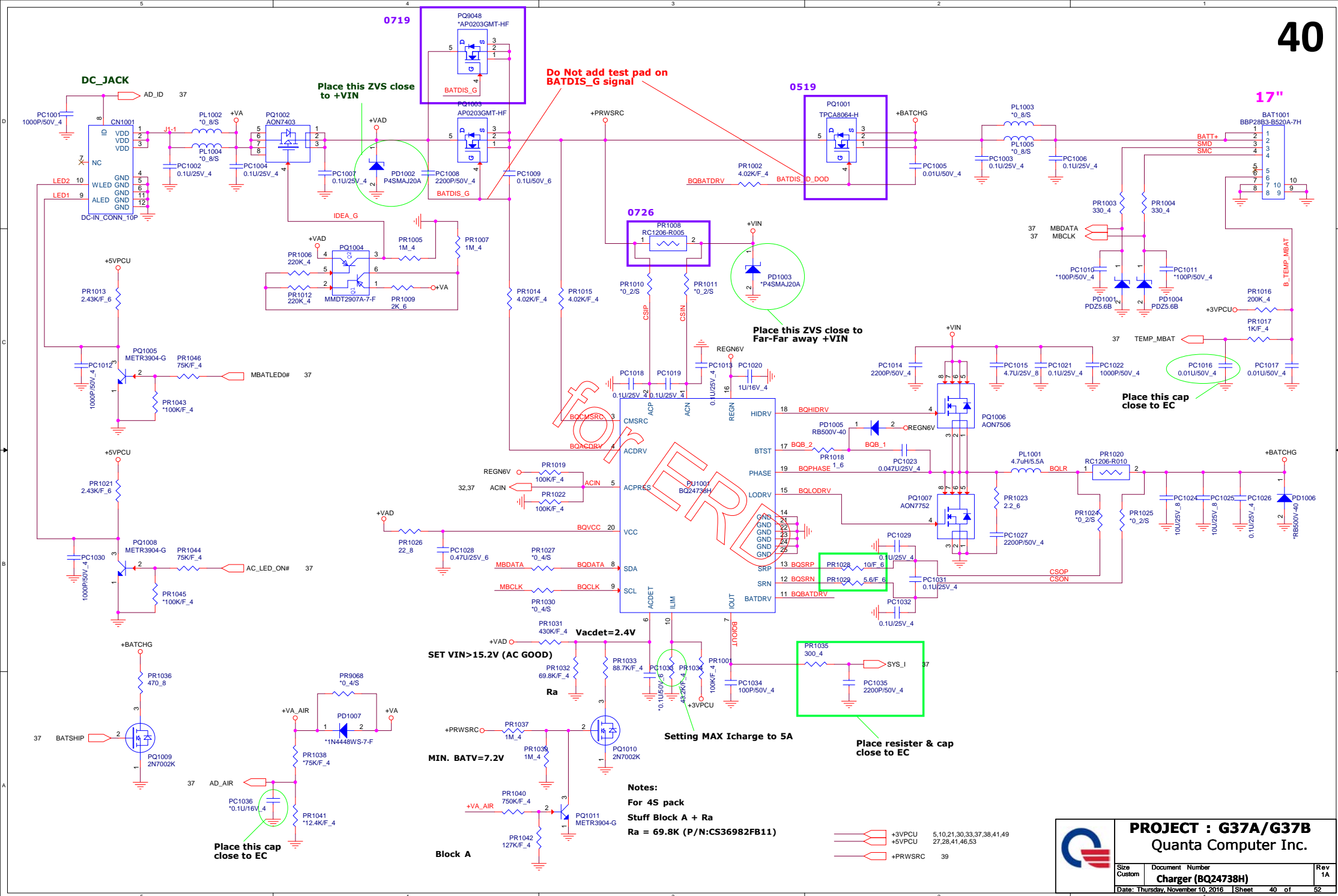
20160308 MV change for EMI request

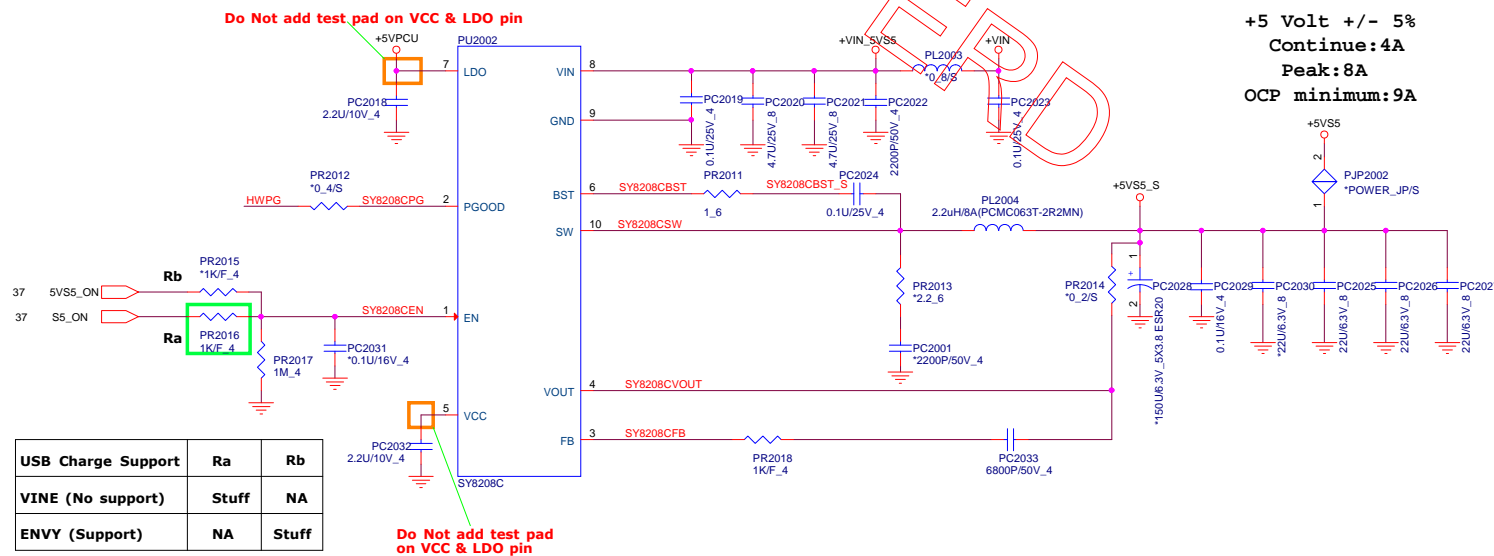
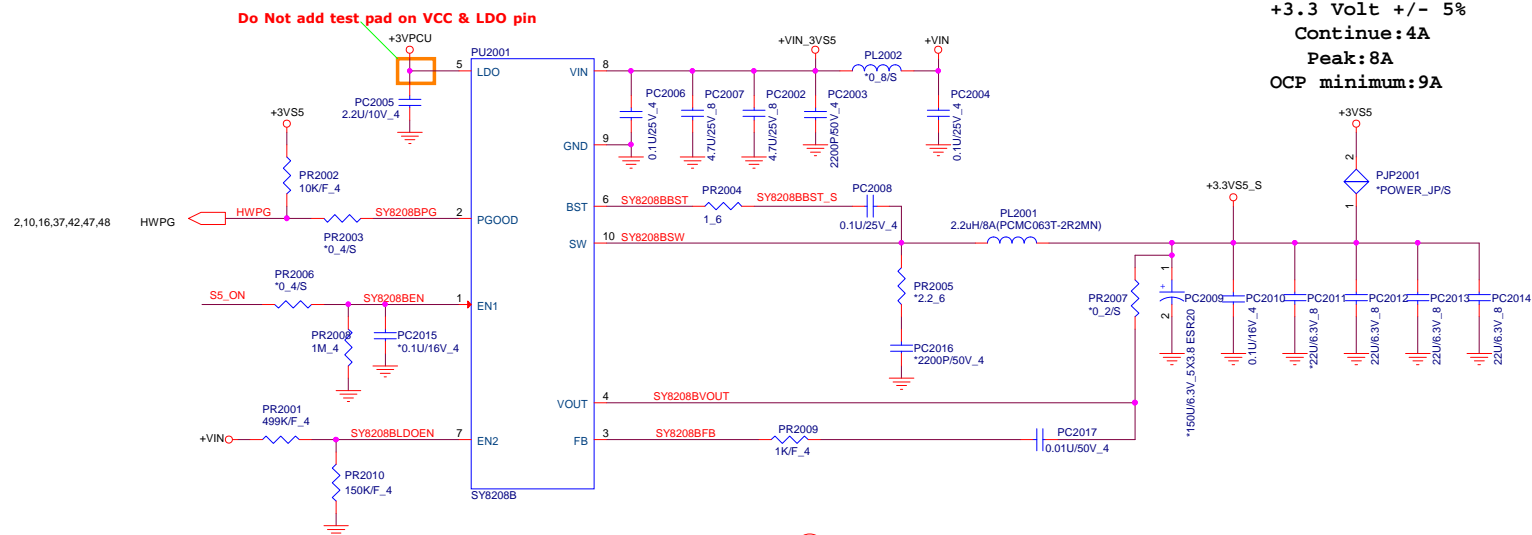
for ERD



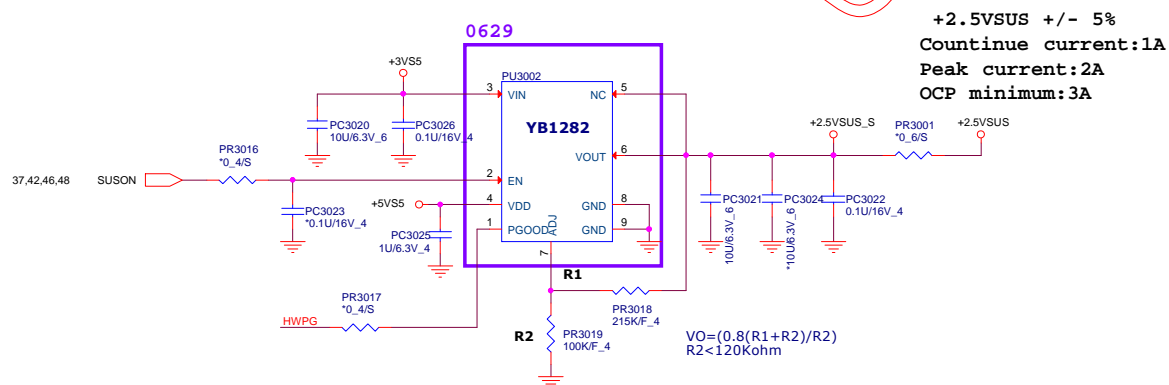
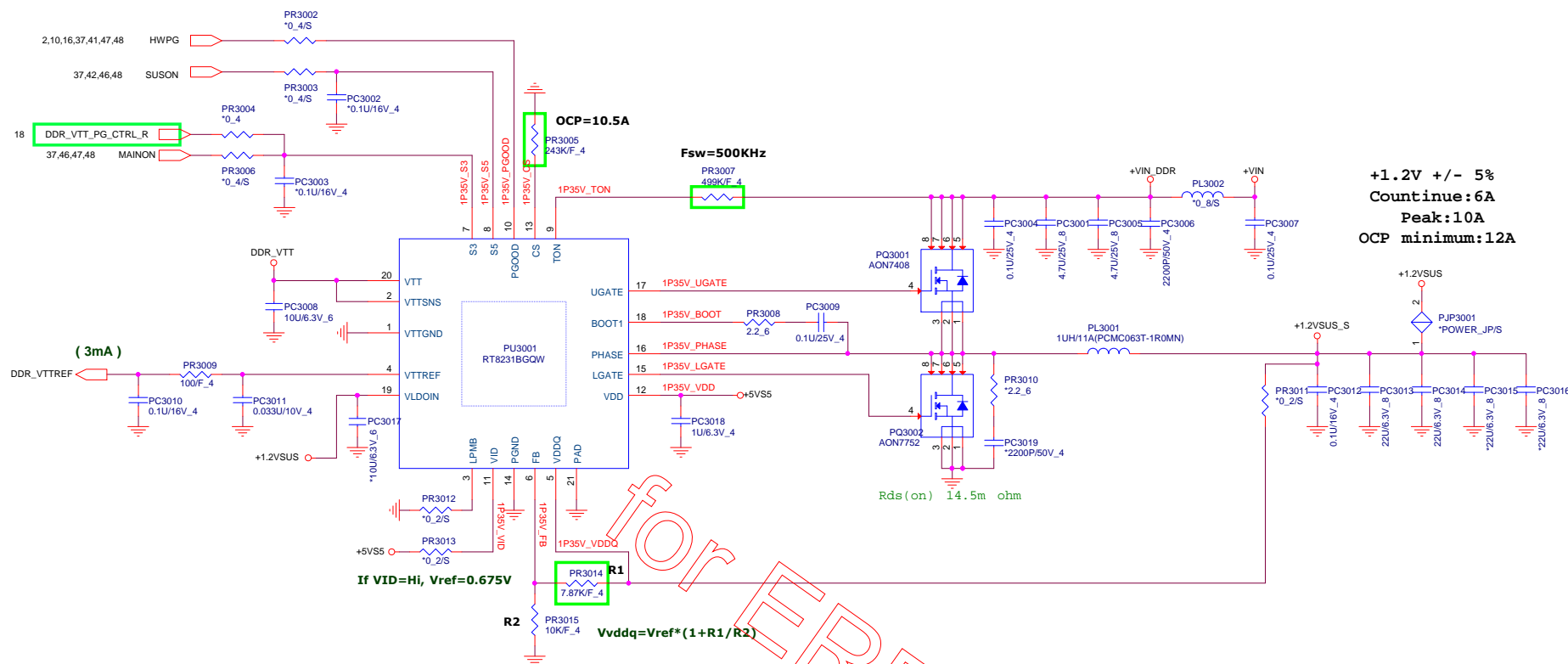
**PROJECT : G37A/G37B**  
Quanta Computer Inc.

|  |                                       |           |
|--|---------------------------------------|-----------|
| Size<br>Custom                                     | Document Number<br><b>RF Solution</b> | Rev<br>1A |
| Date: Thursday, November 10, 2016   Sheet 39 of 52 |                                       |           |





+VIN 26,32,38,39,40,42,43,44,45,46,47,48,49,52  
 +3VSS 10,12,14,16,26,33,37,42,46,47,48  
 +5VSS 10,28,29,30,42,43,44,45,46,47,48,49,50,51,52,53  
 +3VPCU 5,10,21,30,33,37,38,40,49  
 +5VPCU 27,28,40,46,53

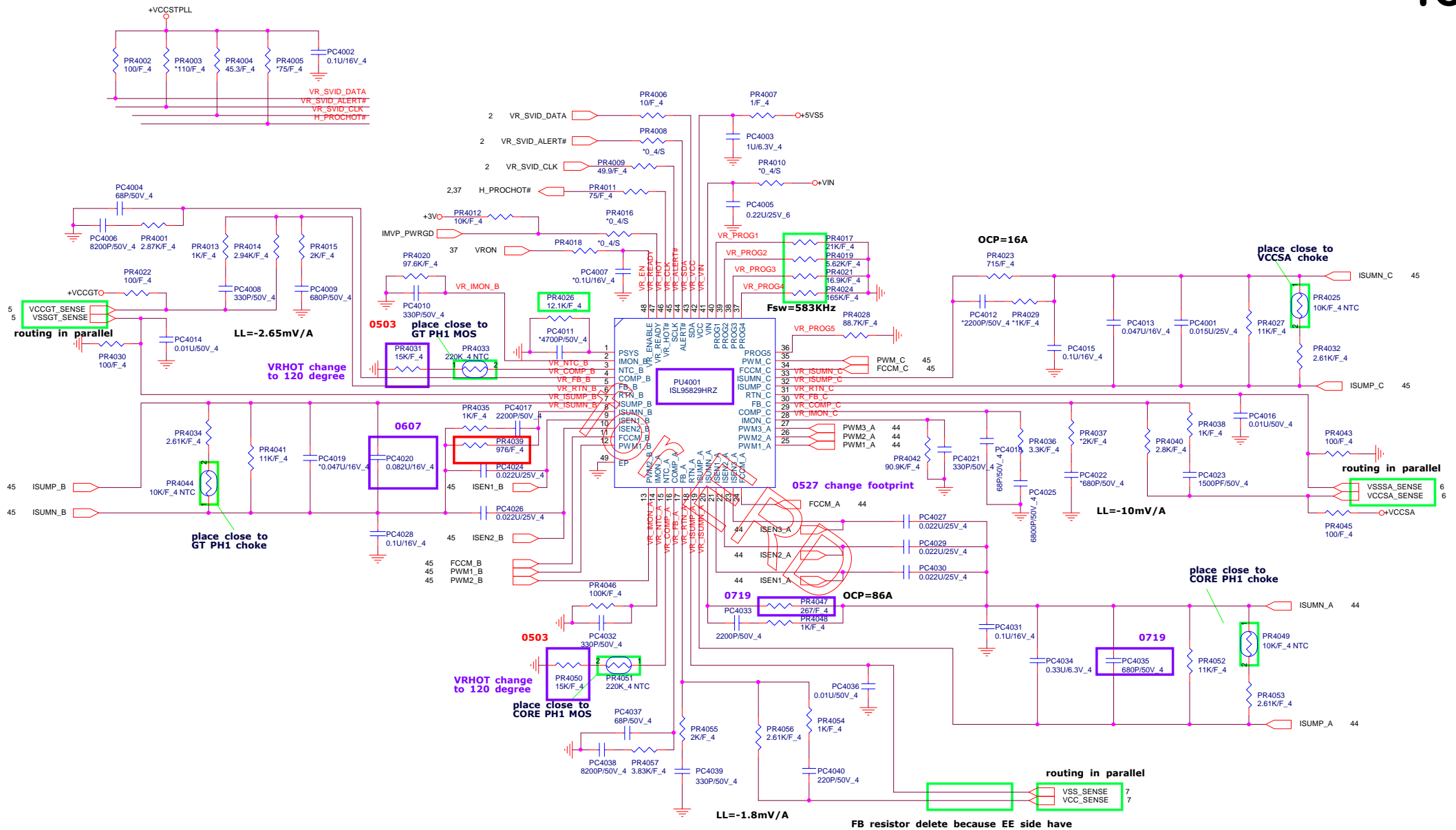


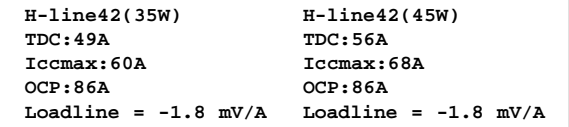
|          |   |
|----------|---|
| +VIN     | 26,32,38,39,40,41,43,44,45,46,47,48,49,52       |
| +5VS5    | 10,26,28,30,41,43,44,45,46,47,48,49,50,51,52,53 |
| +1.2VSUS | 2,6,10,17,18,48,53                              |
| DDR_VTT  | 17,18   |
| +2.5VSUS | 17,18   |



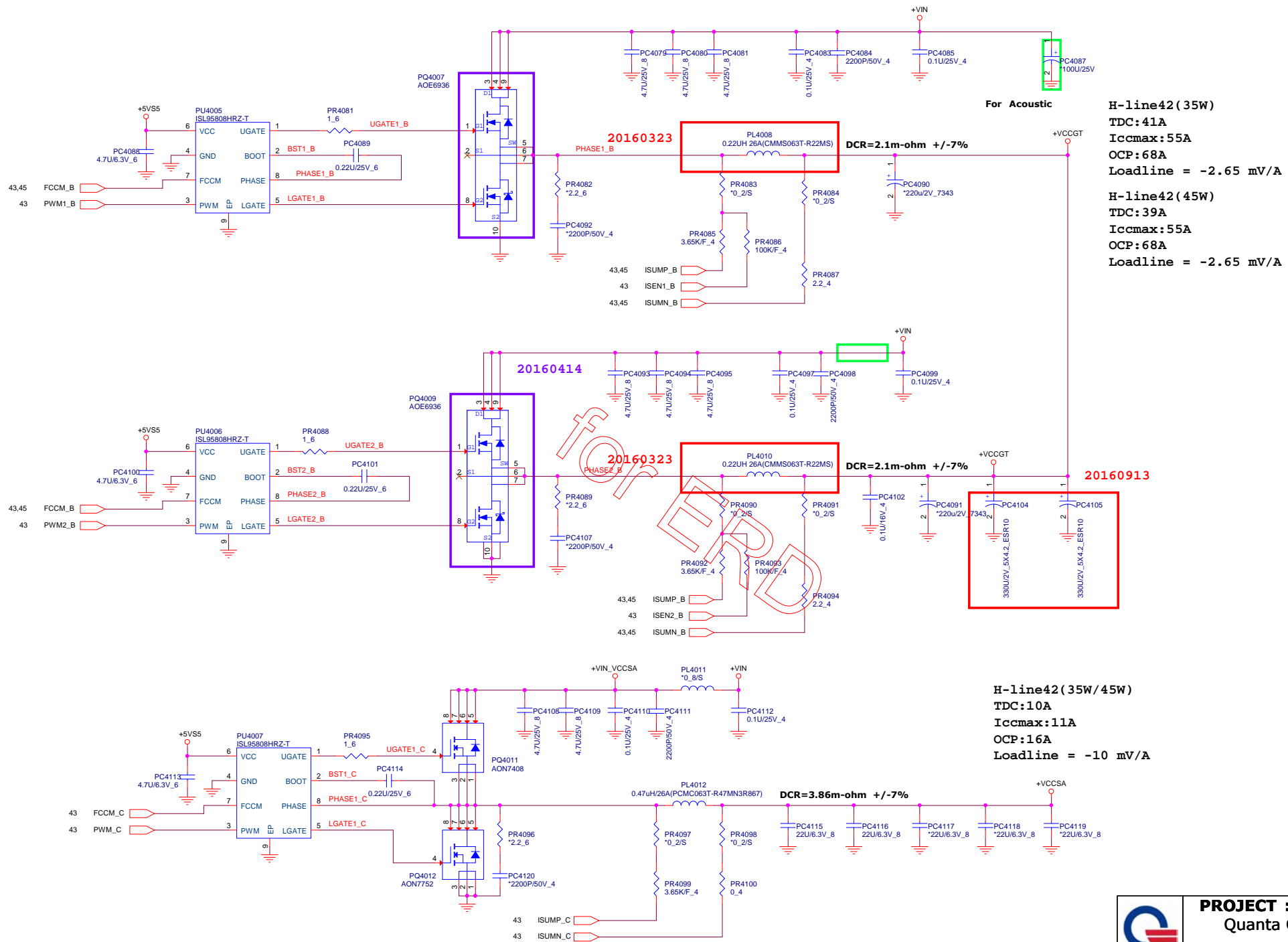
**PROJECT : G37A/G37B**  
Quanta Computer Inc.

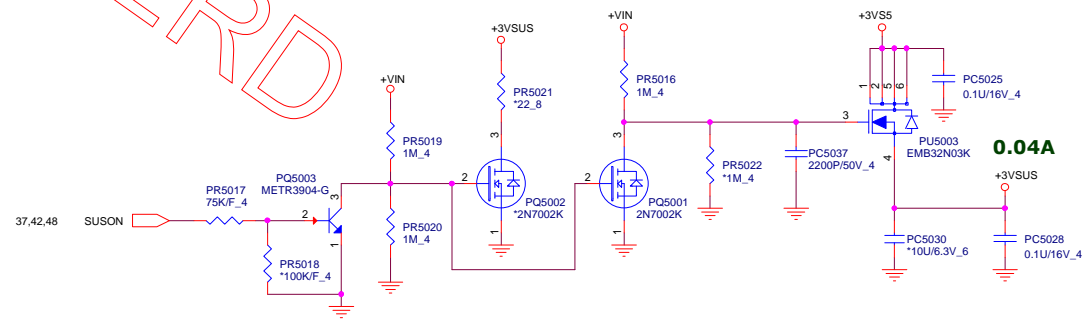
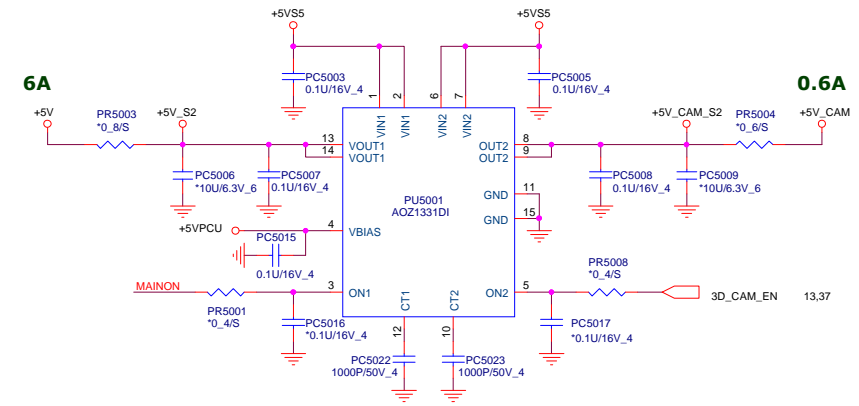
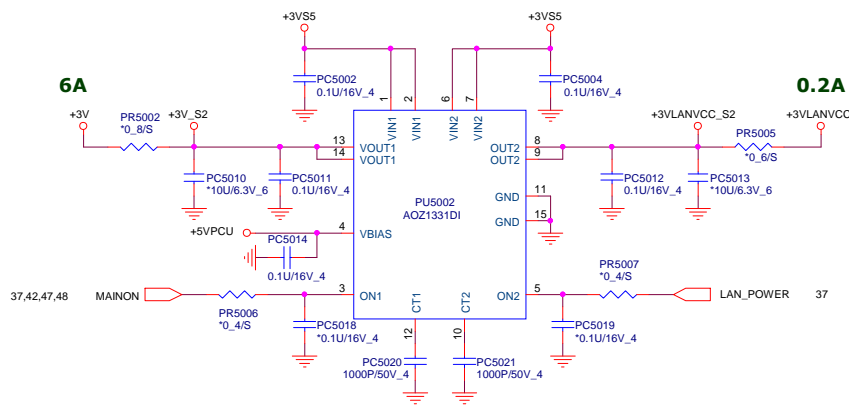
|      |  |           |
|------|--|-----------|
| Size | Document Number<br><b>DDR3 (RT8231B)</b> | Rev<br>1A |
|------|--|-----------|








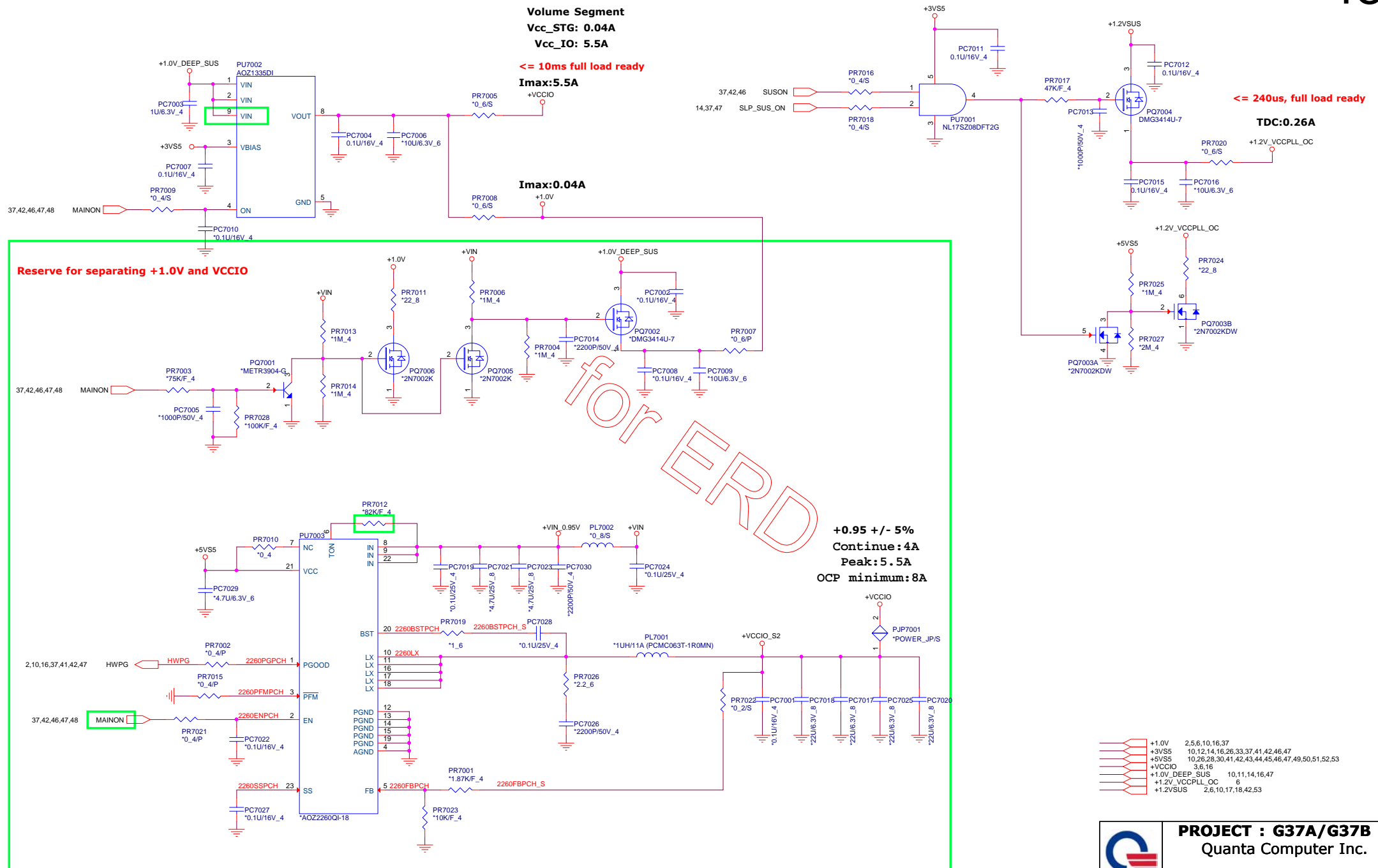





|              |   |
|--------------|---|
| +3V          | 5,9,10,11,12,13,14,16,17,18,26,27,28,29,30,32,33,34,35,36,37,38,43,52 |
| +5V          | 26,27,28,29,31,32,38  |
| +3VS5        | 10,12,14,16,26,33,37,41,42,47,48                                      |
| +5VS5        | 10,26,28,30,41,42,43,44,45,47,48,49,50,51,52,53                       |
| +3VSUS       | 38  |
| +3VLANVCC    | 27,35   |
| +5V_CAM      | 31  |
| +3V_DEEP_SUS | 9,10,12,13,14,16,18   |

|  |   |           |
|--|---|-----------|
|  <b>PROJECT : G37A/G37B</b><br>Quanta Computer Inc. |   |           |
| Size<br>Custom   | Document Number<br><b>Load switch IC (AOZ1331D)</b> | Rev<br>1A |
| Date: Thursday, November 10, 2016   Sheet 46 of 52   |   |           |

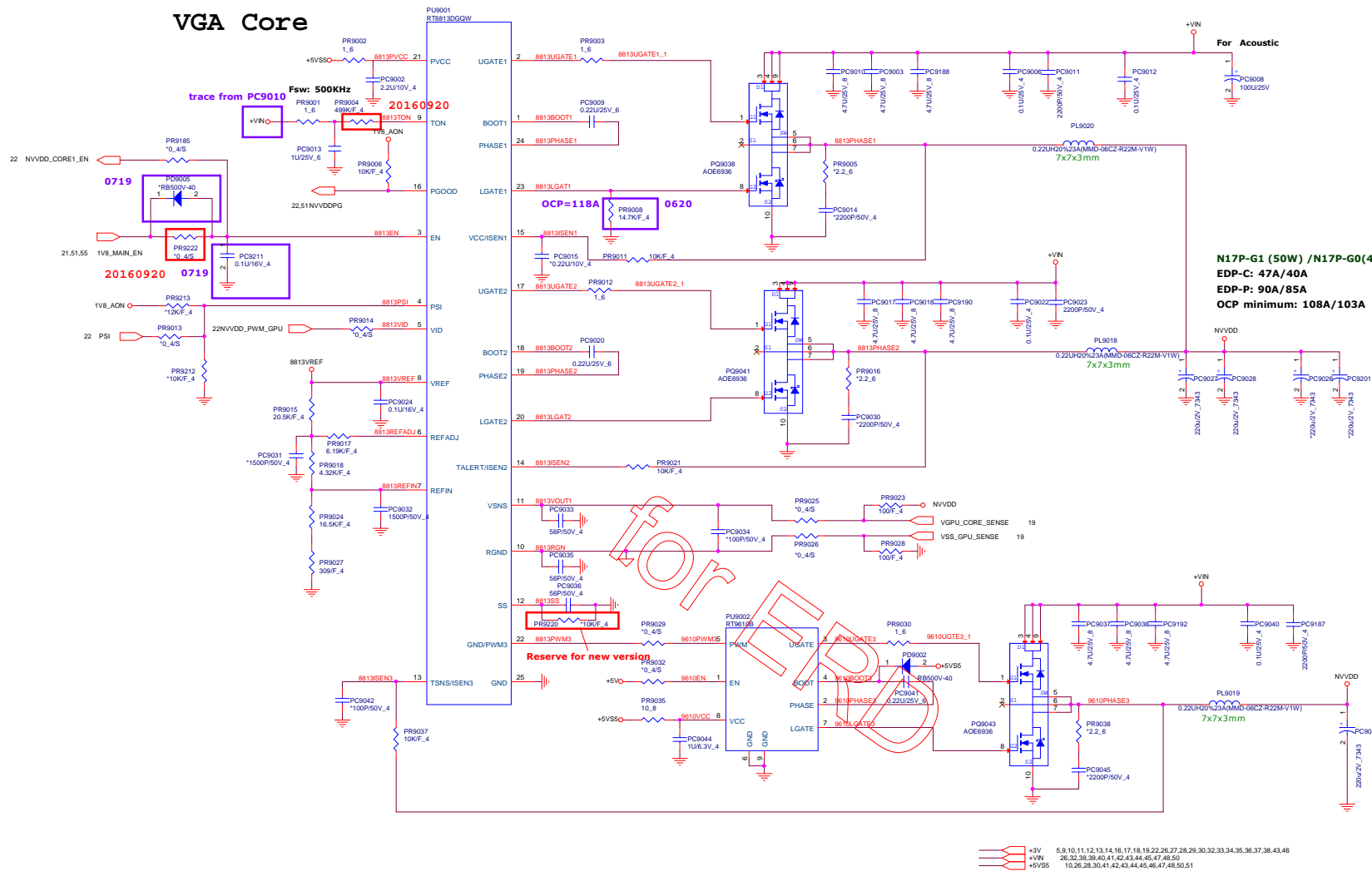




+1.0V 2,5,6,10,16,37  
+3VS5 10,12,14,16,26,33,37,41,42,46,47  
+5VS5 10,26,28,30,41,42,43,44,45,46,47,48,50,51,52,53  
+VCCIO 3,6,16  
+1.0V\_DEEP\_SUS 10,11,14,16,47  
+1.2V\_VCCPLL\_OC 6  
+1.2VSUS 2,6,10,17,18,42,53

|   |                              |       |  |
|---|------------------------------|-------|--|
|  | <b>PROJECT : G37A/G37B</b>   |       |  |
|   | <b>Quanta Computer Inc.</b>  |       |  |
| Size  | Document Number              | Rev   |  |
| Custom  | <b>+1.0V/+VCCSTPLL+VCCIO</b> | 1A    |  |
| Date: Thursday, November 10, 2016   | Sheet 48                     | of 52 |  |

## VGA Core



## NVDDS

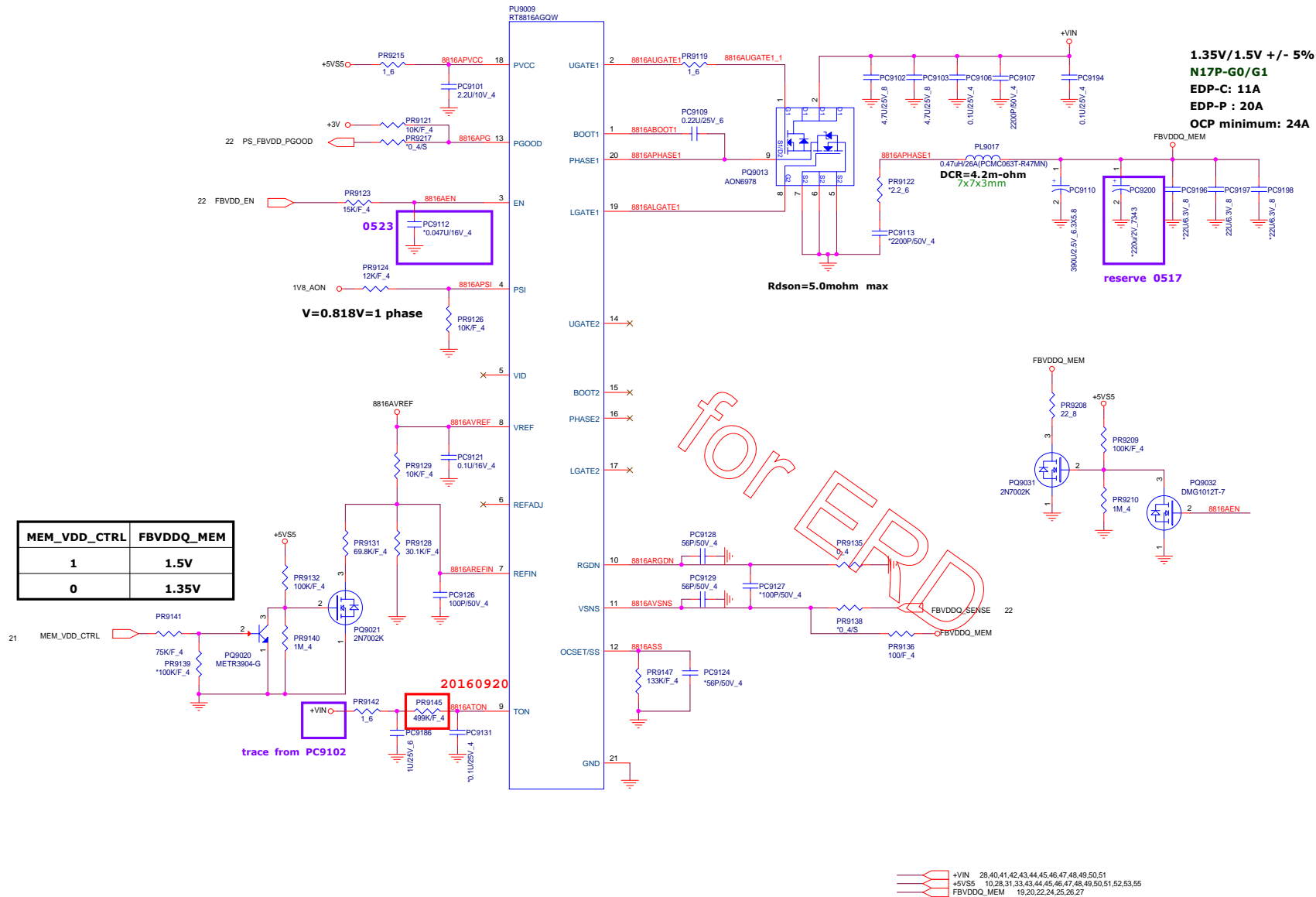
1. Ripple Current:  
Irip=7.79A
2. Ripple Voltage:  
ESR/1=9mohm  
Vrip=70.11mV
3. MOSFET Spec:  
L-side MOSFET: FDP5030  
Rds(ON)=3mohm (Vgs=4.5 V)  
I cont = 25A (T =25 °C)  
I pulse=503A
4. Frequency:  
F=500KHz (PR9224=300k ohm)
5. OCP:  
Set = PR9008 to 14.7K  
Vtrip= PR9008\*10uA-40mV=107V  
Iocp=(Vtrip/Rdson) + Iripple/2  
= 39.565A (1 phase)  
Total OCP=39.565\*3=118.7A (3 phase)

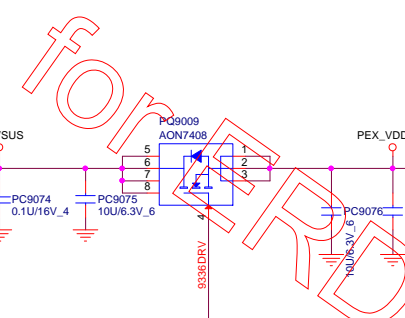






**PROJECT : G37A/G37B**  
Quanta Computer Inc.

| Rev | Docu | Number | Sheet |
|-----|------|--------|-------|
| 1A  | 1    | 1      | 1     |

Date: Thursday, November 10, 2016 11:01 AM





|   |          |   |
|---|----------|---|
|  | +VIN     | 26,32,38,39,40,41,42,43,44,45,47,48,49, |
|  | +3VS5    | 10,12,14,16,26,33,37,41,42,46,47,48     |
|  | +5VS5    | 10,26,28,30,41,42,43,44,45,46,47,48,4   |
|  | +1.2VSUS | 2,6,10,17,18,42,46,48                   |



|                                  |   |                |
|----------------------------------|---|----------------|
| Size Custom                      | Document Number<br><b>+3V/+1.05V_GFX(AOZ1331DI)</b> | Rev<br>1A      |
| Date Thursday, November 10, 2016 |   | Sheet 51 of 52 |

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